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(54) Video signal encoding apparatus

Vorrichtung zur Kodierung eines Videosignals

Dispositif de codage d'un signal vidéo

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- **IEEE TRANSACTIONS ON ACOUSTICS, SPEECH, AND SIGNAL PROCESSING vol. 37, no. 11, November 1989, NEW YORK, US pages 1743 - 1749 , XP000074460 NGAN ET AL 'Adaptive Cosine Transform Coding of Images in Perceptual Domain'**
- **PATENT ABSTRACTS OF JAPAN vol. 13, no. 558 (E-858)12 December 1989 & JP-A-12 31 583**
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- **SIGNAL PROCESSING OF HDTV, PROCEEDINGS OF THE SECOND INTERNATIONAL WORKSHOP ON SIGNAL PROCESSING OF HDTV. L' AQUILA, ITALY , EDITED BY L. CHIARIGLIONE 29 February 1988, AMSTERDAM pages 231 - 238 , XP000075058 CHANTELOU ET AL 'Adaptive transform coding of HDTV pictures'**
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Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a video signal encoding apparatus according to the pre-characterizing part of claim 1.

Description of the Prior Art

If video data converted to digital signals is directly recorded on tape or other recording medium, the volume of data will be so great that it will usually exceed the limit of the data amount that the recording medium can hold. Therefore, when recording a digital video signal on tape or other recording medium, it is necessary to compress it so that the data volume does not exceed the limit. To achieve this, it has been known to compress the video signal by using a high-efficiency encoding apparatus.

One example of such high-efficiency encoding that has been widely used is the orthogonal transform encoding method in which transform coefficients obtained by orthogonal-transforming the original signal are quantized for encoding. This method is known to provide high encoding efficiency. In encoding a video signal by this method, the video signal is first divided into blocks each consisting of $n \times n$ pixels (where n is an integer), an orthogonal transformation is performed on each block to transform it into a transform coefficient representing $n \times n$ frequency regions, and then the transform coefficient is quantized. However, when all blocks are quantized with the same number of bits, adequate image quality can be obtained for the video blocks in flat areas, but noise appears in the video blocks including edge areas since errors are dispersed in the vicinity of the edge areas.

An example of an encoding apparatus that overcomes the above problem is disclosed in Japan Patent Application Laid-Open No. JP-A-2-105792. Fig.1 shows a block diagram of the encoding apparatus disclosed in the Patent Publication. The encoding apparatus shown is described below with reference to Fig.1. A video signal is inputted to a blocking circuit 51 where it is divided into blocks, each block then being supplied to an orthogonal transforming circuit 52 for orthogonal transformation. The transform coefficient obtained by the orthogonal transformation is quantized by a quantizing circuit 53. The quantizing circuit 53 has the ability to perform quantization using a variable number of quantization bits. An edge area detecting circuit 54 is provided to detect the edges of the video signal, while a flat area detecting circuit 55 is provided to determine whether the block represents a flat area. Based on the outputs from the edge area detecting circuit 54 and the flat area detecting circuit 55, a block identifying circuit 56 determines whether the block includes an edge area as well as a flat area, the result of which is fed to the quantizing circuit 53 to determine the number of quantization bits. When the whole block is flat or when the whole block has a complicated structure, it is decided to use a smaller bit code for-quantization since noise is not appreciably visible. On the other hand, if the block includes an edge area as well as a flat area, it is decided to use a higher bit code for quantization to prevent the generation of noise in the flat area. Thus, in the encoding apparatus disclosed in the above Patent Publication, in order to overcome the aforementioned problem, the transform coefficients for blocks including both edge and flat areas are quantized using a higher bit code to reduce the noise and thereby improve the image quality after decoding. The determining factors used to detect the edge or flat areas in a block include a variance within the block, the maximum value of the block, the dynamic range of the block, etc. These factors are collectively referred to as the activity index. In the above prior art encoding apparatus, the number of quantization bits (quantization level) is selected for each block on the basis of the activity index.

The output of the quantizing circuit 53 of Fig.1 is encoded, usually using entropy encoding such as Huffman encoding, into a variable-length code for transmission. The bit length of one block after variable-length encoding varies from block to block, and in the case of a recording medium such as a helical scan digital video tape recorder (VTR) having a fixed track length, it is convenient to grasp the number of data blocks to be recorded per track. Therefore, it is a usual practice to predetermine at least the number of data blocks to be recorded per track. Also, when block correcting codes (e.g., BCH codes, Reed-Solomon codes, etc.) are employed as error-correcting codes, it may be practiced to fix the data length of variable-length code for each error-correcting block. Usually, in encoding of video signals, one field or frame is divided into N segments (where N is an integer), each segment serving as a unit, and the maximum data amount is set for each of the N units.

However, in a channel, such as a digital VTR, in which the data length for the variable-length codes is fixed, the data length of variable-length code may vary from code to code after variable-length encoding depending on the kind of the image processed, and the total code length after variable-length encoding may exceed the fixed length of the channel, resulting in an overflow. If this happens, the transmission will be cut off because of dataflow, and therefore, not only overflown data but also the subsequent data will not be transmitted. This presents the problem of an inability

to correctly perform the decoding of the original signal.

Variable-length encoding of a television image is usually performed in sequence from left to right and from top to bottom of the television screen. Therefore, the problem is that the above-mentioned cutoff is likely to occur in the center of the television screen where the feature elements of the image are contained.

IEEE TRANSACTIONS ON ACOUSTICS AND SPEECH AND SIGNAL PROCESSING; vol. 37, no. 11, November 1989, NY, US, pages 1743-1749, NGAN et al.: "Adaptive Cosine Transform Coding of Images in Perceptual Domain" already discloses a video signal encoding apparatus for compressing and encoding a digital video signal to obtain coded data compressed within a predetermined data amount. This apparatus comprises means for structuring blocks each consisting of a plurality of pixels in the video signal, means for performing an orthogonal transformation on each of the structured blocks to obtain a transform coefficient, means for quantizing the transform coefficient, means for encoding the quantized data to obtain coded data, means for encoding the quantized data to obtain coded data, means for storing the obtained coded data, and means for controlling the quantizing means on the basis of the amount of the coded data stored in the storage means.

PAJP, vol. 12, no. 124 (E 601) shows a picture signal transmission system which obtains a smooth reproducing moving image with improved visual characteristic by dividing both surfaces into plural areas, applying priority to the respective areas and transmitting more information of the area of the higher priority than the information of the area of the lower priority.

PAJP. vol. 12, no. 355 (E 661) describes a picture compressing device which in order to reduce the number of quantizing errors and to shorten the operating time comprises a preprocessing means which pre-processes original picture data and a rearranging section which rearranges an orthogonally transformed output in blocks of the same frequency component.

Further, EP-A-0 322 955 refers to a receiver for a high definition television signal in which the signal prior to transmission is sub-sampled on a block-by-block basis according to the movement. The received sub-sampled signal is applied to a shuffler which shuffles the pixels of blocks in a manner which is the inverse to that performed prior to transmission.

SUMMARY OF THE INVENTION

It is the object of the invention to provide a video signal encoding apparatus capable of fixing the encoded data length to a predetermined length wherein distortions resulting from transmission cutoffs are not easily visible.

This object according to the invention is solved by a video signal encoding apparatus having the features of claim 1. Specific embodiments of this apparatus are defined in claims 2 to 7.

According to the present invention, a video signal encoding apparatus for compressing and encoding a digital video signal to obtain coded data compressed within a predetermined data amount, comprising block structuring means for structuring blocks each consisting of a plurality of pixels in said video signal, transformation means for performing an orthogonal transform on each of the structured blocks to obtain a transform coefficient, quantizing means for quantizing the transform coefficient, encoding means for encoding the quantized data to obtain coded data, storage means having a storage capacity approximately equal to said predetermined data amount, for storing the obtained coded data, and control means for controlling the on/off operation of said encoding means on the basis of the amount of the coded data stored in said storage means, is characterized by shuffling means for shuffling the blocks structured by said block structuring means, so that said blocks may be sequentially supplied to said transformation means starting with the blocks in the center of the screen.

The above and further objects and features of the invention will more fully be apparent from the following detailed description with accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing the configuration of a prior art videod signal encoding apparatus.

Fig. 2 is a diagram showing the configuration of a video signal encoding apparatus comprising a variable length encoding circuit and a buffer memory.

Fig. 3 is a diagram showing an example of encoding during the process.

Fig. 4 is a diagram showing the scanning sequence during encoding.

Fig. 5 is a diagram showing an alternative configuration of the apparatus of Fig. 2.

Fig. 6 is a diagram showing the configuration of a video signal encoding apparatus in accordance with a first embodiment of the invention.

Fig. 7 is a series of diagrams showing in a specific manner the transmission sequences determined by the shuffling circuit shown in Fig. 6.

Fig. 8 is a diagram showing an alternative configuration of the first embodiment.

Fig. 9 is a diagram showing the configuration of a video signal encoding apparatus of a second embodiment.

Fig. 10 is a diagram showing a table of bit code selection for quantization om accordance with the second embodiment.

Fig. 11 is a diagram showing the configuration of an event converting circuit in the second embodiment.

Fig. 12 is a diagram showing an alternative configuration of the second embodiment.

Fig. 13 is a graph showing code length variations equalized by shuffling in the second embodiment.

Fig. 14 is a diagram showing shuffling units for a sample ratio of 4:1:1 in the second embodiment.

Fig.15 is a diagram showing shuffling units for a sample ratio of 4:2:0 in the second embodiment.

Fig.16 is a diagram showing an example of shuffling the second embodiment.

Fig.17 is a diagram showing shuffling units for a sample ratio of 4:1:0 in the second embodiment.

Fig. 18 is a diagram showing the configuration of a video signal encoding apparatus in accordance with a third embodiment of the invention.

Fig.19 is a diagram explaining the operation of shuffling in the third embodiment.

Fig. 20 is a diagram explaining the principle of shuffling in the third embodiment.

Fig. 21 is a diagram showing an example of shuffling the third embodiment.

Fig. 22 is a diagram showing another example of shuffling in the third embodiment.

Fig. 23 is a diagram showing still another example o shuffling in the third embodiment.

Fig. 24 is a diagram showing the configuration of a shuffling circuit in the third embodiment.

In Figure 2, the reference numeral 1 indicates a blocking circuit for dividing the input digital video signal into blocks each consisting of plurality of pixels. Each block is fed from the blocking circuit 1 to a DCT circuit 2. The DCT circuit 2 performs a discrete cosine transform (DCT) on each block and supplies the obtained transform coefficient (DCT coefficient) to a weighting circuit 3. The weighting circuit 3 performs a weighting to each DCT coefficient and supplies the weighted DCT coefficient to a quantizing circuit 4. The quantizing circuit 4 quantizes the weighted DCT coefficient with the number of quantization bits determined by a controller 8, and supplies the quantized DCT coefficient to a variable-length encoding circuit 5 through a switch 7. The variable-length encoding circuit 5 encodes the quantized DCT coefficient into a variable-length code and transfers the variable-length encoded data to a buffer memory 6. The buffer memory 6 is constructed from a RAM or the like and has the storage capacity equivalent to the data length of one track. The switch 7 turns on and off the data input to the variable-length circuit 5. The controller 8 controls the number of quantization bits for the quantizing circuit 4, as well as the switching operation of the switch 7, on the basis of the amount of data stored in the buffer memory 6.

The operation will now be described.

The data obtained by sampling the video signal is divided by the blocking circuit 1 into blocks each consisting of, for example, eight pixels in both horizontal and vertical directions. The DCT circuit 2 performs a DCT on each block, and the obtained DCT coefficient is then performed a weighting by the weighting circuit 3. At this time, the weighting is performed so that weighting factors for DOT coefficients in higher frequency regions will be smaller values. This is because the visual resolution drops for higher frequency regions, allowing high-efficiency encoding without noticeable degradation. Next, the weighted DCT coefficient is quantized by the quantizing circuit 4. Quantized n-bit data may be expressed as shown in Fig.3, for example. This data is encoded by the variable-length encoding circuit 5 into a variable-length code by performing one-dimensional scanning as shown in Fig.4. The variable-length encoding circuit 5 is a circuit for encoding data into a code whose length depends, for example, on the string of zeros (zero run length) and nonzero value, and usually, the Huffman encoding and like methods are widely used. The output of the variable-length encoding circuit 5 is stored in the buffer memory 6 for transfer to the transmission channel.

However, the length of the variable-length code outputted from the variable-length encoding circuit 5 varies according to the image pattern and, depending on the situation, may exceed or may not reach the maximum transmissible code length. The controller 8 predicts an occurrence of excess data by comparing the address value being written in the buffer memory 6 with the limit data length, and outputs signals to control the number of quantization bits for the quantizing circuit 4 and the switching operation of the switch 7.

Therefore, even if the data volume instantaneously increases at a particular portion of the image on the television screen, the buffer memory 6 can provide a sufficient capacity for data storage, and there arises no situation that results in an overflow or that causes the controller 8 to direct transmission cutoff.

Fig.5 is a block diagram showing an alternative configuration. In this alternative configuration, the controller 8 controls only the switching operation of the switch 7. The preferred embodiment of the present invention will now be described with reference to the accompanying drawings.

(Embodiment 1)

Fig. 6 is a block diagram showing the configuration of the first embodiment, the reference numerals designating corresponding parts being the same as those in Fig.2. In the first embodiment, there is provided between the blocking

circuit 1 and the DCT circuit 2 a shuffling circuit 9 by which the blocks entered from the blocking circuit 1 are shuffled so that the encoding of image data is performed starting preferentially from the center of the television screen, the thus shuffled blocks being supplied to the DCT circuit 2.

Fig.7 shows the shuffling sequences performed by the shuffling circuit 9. Fig.7(a) shows an example in which the shuffling is performed in such a manner as to spiral outward from the center of the screen. Fig.7(b) shows an example in which the shuffling is performed in the vertical direction across the screen starting from the center and alternately moving toward both ends of the screen. Furthermore, Fig. 7(c) shows an example in which the shuffling is performed in the horizontal direction across the screen starting from the center and moving alternately toward the top and bottom of the screen.

Thus, in the first embodiment, the encoding is performed starting preferentially from the center of the screen, and therefore, if data transmission is cut off because of an occurrence of excess data, since the cutoff occurs in an edge portion of the screen, the distortion resulting from the cutoff is less visible.

The shuffling sequences performed by the shuffling circuit 9 are not limited to the methods shown in Figs.7(a), (b), and (c), but instead, random numbers may be used. For example, the television screen may be divided into five sections, as shown in Fig.7(d), and the shuffling sequence within each section may be determined by random numbers, starting from the center section and moving alternately toward both sides of the screen.

Fig.8 is a block diagram showing an alternative configuration of the first embodiment. In this alternative configuration, the controller 8 controls only the switching operation of the switch 7.

(Embodiment 2)

The following describes the second embodiment in which the number of quantization bits is decided on the basis of the activity index of each block and the number of event occurrences. Variable-length encoding means assigning codes of varying lengths according to data occurrence. When the data count is increased (i.e. when tens of thousands to hundreds of thousands of codes are viewed), the bias in the code amount decreases. Further, when tens of thousands to hundreds of thousands of codes are viewed, it has been confirmed by simulation that the average code length per event (one event means one occurrence of zero run length and nonzero value) is stable approximately between 5 to 7 bits. Using this property the other way around, the entire code amount can be predicted fairly accurately by counting the number of events. The second embodiment uses such property of variable-length codes to predict the code amount and decide the number of quantization bits based on the predicted value.

Fig.9 is a block diagram showing the configuration of the second embodiment, wherein the same reference numerals a those in Fig.2 refer to the same or corresponding parts for which the description is omitted herein. The quantizing circuit 4 quantizes the weighted DCT coefficient with the number of quantization bits decided by a quantization bit number deciding circuit 14 and supplies the quantized DCT coefficient to the variable-length encoding circuit 5. The variable-length encoding circuit 5 encodes the quantized DCT coefficient into a variable-length code, the variable-length code data then being transferred to a buffer memory 11 constructed from a RAM or the like. The variable-length encoding circuit 5 also supplies data to a data restructuring circuit 10. The data restructuring circuit 10 restructures the data from the variable-length encoding circuit 13. The variable-length encoding circuit 13 encodes the input data into a variable-length code for transfer to a buffer memory 15 constructed from a RAM or the like. A switch 12 selects data output between the buffer memories 11 and 15. The variable-length encoding circuit 5 comprises a zero run counter 31 for counting zero runs in the output of the quantizing circuit 4, an event counter 32 for counting the number of event occurrences by the count value of the zero run counter 31, an event converting circuit 33 for converting an event, as hereinafter described, in accordance with the count value of the event counter 32, and a variable-length encoder 34 for encoding the output of the event converting circuit 33 into a variable-length code.

The operation will now be described. Fig. 10 shows an example of quantization bit code selection. In the second embodiment, the predicted memory usage in the buffer memory 11 and the activity index are taken as the deciding factors. Thus, when it is predicted that the usage of the buffer memory 11 is nearing its full capacity, the number of quantization bits is reduced, so that the probability increases that post-quantization values become zero. As a result, the code length after variable-length encoding decreases per pixel. In this manner, the code amount decreases as the buffer memory 11 nears its full capacity, thus providing effective control against overflow. When the situation has reached or is expected to reach the critical point at which an overflow occurs, the variable-length encoding by be cut off at a point at the high frequency side.

In the variable-length encoding circuit 5, the zero run counter 31 for counting zero runs is usually provided to count the contents of events (zero run length and nonzero value) preparatory to variable-length encoding. The zero run counter 31 notifies the occurrence of a code for every event to the event counter 32 which counts the number of events to predict the code amount to be generated. For example, the average number of events per block is obtained, which is fed back to the quantization bit number deciding circuit 14 which, considering both the average number and the activity index, decides the number of quantization bits as shown in Fig.10, thereby controlling the code amount.

Independently of the above feedback, the number of events is counted by the event counter 32, and after the total number of events has been counted, the event converting circuit 33 performs a control on the code amount. When it is predicted by the event counter 32 that the code amount is likely increased, for example, the control is performed in the following manner. There are some events whose nonzero value may be reduced to zero if the value is divided by 2 and truncated to a whole number. This occurs when the nonzero value is 1. When a new zero value occurs in an event, the run length of that event is added to the run length of the next event and 1 is further added to this sum to provide the run length of a new event. This can be described by the following specific example.

Suppose, for example: the kth event has a run length of 5 and a nonzero value of 6; the (k+1)th event has a run length of 2 and a nonzero value of 1; and the (k+2)th event has a run length of 7 and a nonzero value of 17.

In this example, if the control is performed as a result of code amount prediction so as to reduce the code amount, the following results will be obtained.

The kth event will have a run length of 5 with a nonzero value reduced to 3;
the (k+1)th event will have a run length of 2 with a nonzero value reduced to 0; and
the (k+2)th event will have a run length of 7 with a nonzero value reduced to 8.

Since, at this time, a new zero value occurs in the (k+1)th event, the (k+2)th event is combined with the (k+1)th event to create a new (k+1)th event. The new (k+1)th event has a run length of 10, which is given by 2 + 7 + 1, and a nonzero value of 8. The old (k+3)th event is now a new (k+2)th event, the old (k+4)th event is now a new (k+3)th event, and thus, new events are sequentially created, reducing the number of events by the number of newly generated zero values.

Fig. 11 shows the internal configuration of the event converting circuit 33 which performs the above-described operation. The event converting circuit 33 comprises: a delay circuit 35 for outputting the input run length with a delay of one event; an adder 36 which adds the output of the delay circuit 35 to the input run length and further adds 1 to this sum; a switch 37 that can be switched between two input terminals, one terminal being supplied with the output of the delay circuit 35 and the other being supplied with the output of the adder 36; a divider 38 which divides the input nonzero value by 2 and truncates the result to a whole number; a zero judging circuit 39 which judges if the output of the divider 38 is zero or not and which, when the output is zero, issues a control signal to the switch 37 and, when the output is not zero, directly outputs the nonzero value; and a delay circuit 40 for outputting the input nonzero value with a delay of one event. When the control signal is given from the zero judging circuit 39, the switch 37 selects the output of the adder 36 and, when the control signal is not given, is selects the output of the delay circuit 35.

The provision of the above configured event converting circuit 33 offers the advantage, for example, that the number of quantization bits, once set for the quantizing circuit 4, can be easily changed using only one zero run counter. Without the event converting circuit 33, two zero run counters, one for prediction of the variable-length code amount and the other for use after changing the number of quantization bits, would be required.

Dividing nonzero values is not an essential element for the operation of the event converting circuit 33; it will also be possible to change the contents of an event by forcibly converting to zero a nonzero value whose absolute value is smaller than a value 1. The event conversion does not necessarily have to be performed uniformly on each block, but may be performed adaptively with emphasis, for example, on portions quantized with higher bit codes by the quantizing circuit 4 or on high frequency components. The event conversion using the 1/2 division is equivalent to changing the number of quantization bits from n bits to (n-1) bits.

Fig. 12 is a block diagram showing an alternative configuration of the second embodiment. In this configuration, a code amount counter 30 for counting the code amount is used instead of the event counter 32 in Fig. 9. The code amount counter 30 counts the generated code amount from the zero run length and nonzero value supplied from the zero run counter 31. At completion of each block, the number of bits such as EOB (end of block, a character that indicates the completion of a block) are added to the counted amount, which is divided by the number of blocks already counted to predict the entire code volume to be generated.

Data that has not been transmitted because of generation of new zeros by the event converting circuit 33 is restructured by the data restructuring circuit 10. If the code amount has failed to reach the predicted value, the restructured data can be encoded as additional data to provide further accurate control. Such additional data is encoded by the variable-length coding circuit 13 and stored in the buffer memory 15, and if the output of the buffer memory 11 falls short of the maximum transmissible code amount, the additional data stored in the buffer memory 15 is transmitted by time-multiplexing through the switch 12, thus enabling the additional data to be transmitted up to the maximum transmissible limit.

On the other hand, when the code amount predicted by the event counter 32 or the code volume counter 30 exceeds the maximum transmissible limit, DCT coefficients with smaller absolute values are cut off in ascending order of the absolute value, because DCT coefficients with smaller absolute values less affects the image quality when cut off. Therefore, counting the number of events having DCT coefficients with smaller absolute values is important in grasping the code amount after code amount control. More specifically, if the number of events having DCT coefficients with absolute values 1, 2, or 3 is counted separately by the event counter 32 or the code amount counter 30 and the

event conversion is performed using this number information in conjunction with the result of code amount prediction, further accurate control of the code amount can be achieved.

That is, the events with an absolute value 1 are converted to non-transmission events by the above-mentioned 1/2 division, and by accurately grasping the number of such non-transmission events, it is possible to increase the control accuracy. For example, in such cases where events with an absolute value 1 seldom occur but events with absolute values 2 or 3 frequently occur, it becomes necessary to create non-transmission events using a 1/4 division, in which case the event converting circuit 33 should be directed to perform a 1/4 division or to forcibly convert the events with absolute values 1, 2, or 3 to non-transmission events. This serves to further enhance the control accuracy.

When recording data on a VTR tape using the above described control, the code amount greatly varies depending on the image pattern to be recorded, as previously noted. It is also noted previously that it is convenient to fix the data length to a length calculated by dividing the track length by an integer. It is usually most convenient to fix the data length by dividing one field or one frame or m frames into n units. Fig.13, for example, shows the generated code amount when one frame is divided into 10 units. The symbol -Δ- in Fig.13 represents the code amount. As shown, four out of the 10 units largely exceeds the transmissible limit, while the other six units are far below the limit. Since the cutoff control is exercised on the four units to a large extent, the code amount has to be reduced, sacrificing the signal-to-noise ratio to a certain degree, while on the other hand, an improvement in the signal-to-noise ratio is expected for the remaining six units with the addition of additional data, etc. When the code amount is controlled between the units in accordance with the second embodiment, such a bias in the code amount distribution can be disregarded since the code amount overflown from the four units can be transmitted using the other six units (actually, using units in the next frame).

However, processing covering too many units only serves to complicate the hardware configuration and does not provide worthwhile advantages. It is therefore important to devise so that the processing will be completed within each unit. That is, it is important to minimize the bias in the code amount within each unit. One approach to this is to equalize the generated code amount between the units by shuffling the blocks so that any given DCT block and four DCT blocks most adjacent to the given DCT block belong to different units. The code amount generated as a result of such shuffling is shown by the symbol -O- in Fig.13. As can be seen from Fig.13, the shuffling has served to substantially equalize the generated code amount. Controlling the code amount within each unit after equalizing is extremely advantageous in terms of the following points. Since the code amount control is performed only within each unit, the hardware is very simple in construction. Even when the code amount control is performed within each unit, there occurs no need to reduce the rate for a particular portion within one frame, as a result of which degradation in the signal-to-noise ratio is prevented from concentrating on a particular portion on the screen.

When special replay modes are considered, it will be more convenient if the code amount is controlled after performing the above-mentioned shuffling by grouping together DCT blocks of the chrominance signal having a fewer number of samples. More specifically, when the sample ratio between the luminance and chrominance signals is 4:1:1, for example, four horizontally successive DCT blocks as shown in Fig.14 are grouped into a shuffling unit and shuffling is performed on this unit, after which the code amount is controlled within this unit. In the case of special replay modes, some blocks may not be reproducible, but when shuffling is performed on the above configured unit, reproduction is possible with both the luminance and chrominance signals balanced. Without such shuffling, the second DCT block from left of the luminance signal, for example, may be dropped, resulting in serious degradation in special replay mode image quality.

Further, when the sample ratio between the luminance and chrominance signals is 4:2:0 (color line sequential processing), for example, the above-described shuffling is performed by grouping two horizontally adjacent and two vertically adjacent DCT blocks into one shuffling unit. With this grouping, the area size that one DCT block of the chrominance signal takes on the screen becomes equal to the shuffling unit of the luminance signal. With this as one shuffling unit, the shuffling as shown in Fig.16 is performed. Fig.16 shows an example of shuffling in the case of the shuffling unit shown in Fig.15 when the sample ratio between the luminance and chrominance signals is 4:2:0 and when one field is divided into five units. Fig.17 is an example of shuffling when the sample ratio between the luminance and chrominance signals is 4:1:0.

(Embodiment 3)

When a plurality of blocks is grouped into a unit, has been a usual practice to perform encoding unit by unit starting from a particular position on the screen (e.g. from the upper left of the screen). Therefore, the code amount varies largely from unit to unit, and there arises the problem that the transmission efficiency decreases when the upper limit of data amount is set to match the units having a larger code amount. The third embodiment is provided aiming at overcoming such a problem.

Fig.18 is a block diagram showing the configuration a video signal encoding apparatus in accordance with the third embodiment. In Fig.18, the reference numerals 2, 3, 4, and 5 designate a DCT circuit, a weighting circuit, a

quantizing circuit, and a variable-length encoding circuit, respectively. These circuits are identical to those shown in Fig.9. At the front stage of the DCT circuit 2, there is provided a blocking/shuffling circuit 41 for dividing a digital video into blocks of a plurality of pixels and shuffling the thus obtained blocks. The block data is supplied from the blocking/shuffling circuit 41 to the DCT circuit 2. The quantizing circuit 4 quantizes the weighted DCT coefficient with the number of quantization bits decided by a quantization bit number deciding circuit 43 and supplies the quantized DCT coefficient to the variable-length encoding circuit 5. The variable-length encoding circuit 5 encodes the quantized DCT coefficient into a variable-length code and supplies the variable-length code data to a buffer memory 42.

The operation will now be described.

A digital video signal is inputted in scanning line sequence to the blocking/shuffling circuit 41 where the signal is divided into blocks of n × n pixels within one field or one frame and then shuffled in accordance, for example, with the shuffling format shown in Fig.19. One block in Fig.19 corresponds to one DCT block and the outer frame corresponds to that of the television screen. When the luminance signal conforming to the NTSC system is sampled at a rate of 13.5MHz, for example, the effective scanning area per frame covers 720 pixels in the horizontal direction and 486 pixels in the vertical direction. When one frame is divided into blocks of 8 × 8 pixels, for example, there remain six pixels each in the vertical direction; therefore, it is supposed here to encode the picture signal for 720 × 480 pixels, discarding the data for the three horizontal scanning lines from the top and bottom of the screen. Since the video signal is divided into blocks of 8 × 8 pixels, this means 90 × 60 blocks, i.e., 5,400 blocks in total. That is, when the block address in the horizontal direction within one frame is denoted as I and that in the vertical direction as J, I is expressed as $1 \leq I \leq 90$ and J as $1 \leq J \leq 60$.

Furthermore, the 5,400 blocks are grouped into N units. In Fig.19, N = 5, and the alphabetic characters in A1, B1, etc. assigned to each block indicate the names of the units. Since N = 5, there are five unit names A to E. The numeric parts in A1, B1, etc. are numbers indicating the encoding sequence within each unit.

In Fig.19, encoding is performed, as a general rule, from left to right and from top to bottom of the screen. In the example shown, since there are 90 blocks in the horizontal direction, the second line from top in Fig.19 begins with the number 19 which is given by dividing 90 by N (= 5) and adding 1 to the quotient. Therefore, the block address (i, j) for the kth encoding in the uth unit can be expressed by the following equation (1) (provided that (1, 1) indicates the top left corner of the screen and (90, 60) the bottom right corner). .pa

$$\left.\begin{aligned} i &= N \times \mathrm{mod}\left(k-1, \frac{90}{N}\right) \\ &\quad + \mathrm{mod}\left(u + \left[\frac{(k-1) \times N}{90}\right] - 1, N\right) + 1 \\ j &= \left[\frac{(k-1) \times N}{90}\right] + 1 \end{aligned}\right\} \quad \ldots (1)$$

[a]: Largest integer not exceeding a

For example, when u = 2 and k = 20, the block address is given by:

$$i = 5 \times \mathrm{mod}(20 - 1, 18) + \mathrm{mod}[2 + [(19 \times 5)/90] - 1,$$

$$5] + 1 = 5 \times 1 + \mathrm{mod}(2, 5) + 1 = 5 + 2 + 1 = 8$$

$$j = [(19 \times 5)/90] + 1 = 2$$

Thus, the block address (8, 2) is obtained. Also, u = 2 indicates the unit name is B, and in Fig. 19, the address (8, 2) designates the block B20. Likewise, the address of the block C57, for example, can be found as follows:

$$I = 5 \times \mathrm{mod}(57 - 1, 18) + \mathrm{mod}[3 + [(56 \times 5)/90] - 1,$$

$$5] + 1 = 5 \times 2 + \mathrm{mod}(3 + 3 - 1,$$

$$5) + 1 = 10 + 0 + 1 = 11$$

$$j = 4$$

which gives the address (11, 4). That is, Fig.19 shows the arrangement of blocks after performing shuffling as expressed by the equation (1).

After the above shuffling, each block is sequentially fed to the DCT circuit 2 for a DCT transform and is then performed a weighting by the weighting circuit 3. The quantization bit number deciding circuit 43 calculates the activity index of each block, on the basis of which the number of quantization bits is decided for the block, the information being fed to the quantizing circuit 4. The weighted DCT coefficient is quantized by the quantizing circuit 4 using the number of quantization bits thus decided, and the quantized data is then encoded by the variable-length encoding circuit 5 using such methods as Huffman encoding, the encoded data being transferred to the buffer memory 42 for storage therein.

As the above shuffling, the patterns represented by the blocks to be coded are randomly dispersed, and therefore, the code length is equalized between the units when the number of blocks is greater than a certain degree. According to the simulation conducted by the inventor, it has been found that, when the units are assigned by shuffling as shown in Fig.19, the dispersion value indicating the dispersion of the code amount is reduced to 1/5 to 1/10, compared to when a particular position on the screen is grouped together in a unit without shuffling.

Next, the features of this shuffling will be considered. When considering the effects that the shuffling has on the code amount, the point is to avoid concentrating the blocks of the same pattern in the same unit, which leads to the following point when considered in conjunction with pixels. Blocks neighboring an attention block often have similar patterns, therefore, processing is performed to assign neighboring blocks to different units. This processing is described below using the concept of neighborhood.

Each of the nine squares in Fig.20 represents a DCT block. There are eight blocks (A to F in Fig.20) that neighbors an attention block. These blocks are referred to as the eight neighboring blocks, of which the four blocks A, B, C, and D that are most adjacent to the attention block are called the four neighboring blocks. Referring back to Fig.19, it can be seen that when attention is given to a given block, none of its four neighboring blocks belong to the same unit as the attention block. Of its eight neighboring blocks, there are only two blocks that belong to the same unit. The four neighboring blocks that are spatially most adjacent to the attention block are thus made to belong to different units in order to prevent similar patterns from being concentrated in one unit. This serves to equalize the code amount.

This effect can be achieved not only by the equation (1) but by many other methods. Figs.21 to 23 show only a few examples of the many methods. In the examples of shuffling shown in Figs.21 to 23, there are no four neighboring blocks that belong to the same unit. The block address (i, j) in Fig.21 is expressed by the following equation. .pa

$$i = \left[\frac{\mathrm{mod}(k-1, 90)}{N}\right] \times N + \left[\frac{N+1}{2}\right] + (-1)^{\mathrm{mod}(k,N)} \times \left[\frac{\mathrm{mod}(k, N)}{2}\right]$$

$$j = \mathrm{mod}(\mathrm{mod}(k-1, 90) + u - 1, N) + 1 + N \times \left[\frac{k-1}{90}\right]$$

For example, to find the address of the block D98, since u = 4 and k = 98,

$$i = [\{\mathrm{mod}(97, 90)\}/5] \times 5 + 3 + (-1)^3 \times [\{\mathrm{mod}(98, 5)\}/2] = 5 + 3 - 1 = 7$$

$$j = \mathrm{mod}\,(7 + 4 - 1, 5) + 1 + 5 \times 1 = 0 + 1 + 5 = 6$$

which gives the address (7, 6). The block address (i, j) in Fig.29 is expressed by the following equation.

$$i = \mathrm{mod}(\mathrm{mod}(k-1, 90) + u, N)$$

$$+[\frac{\mathrm{mod}(k-1, 90)}{N}] \times N$$

$$j = [\frac{k-1}{90}] \times N + [\frac{N+1}{2}] + (-1)^{\mathrm{mod}(k-1, N)} \times [\frac{\mathrm{mod}(\mathrm{mod}(k-1, 90), N) + 1}{2}]$$

For example, to find the address of the block E102, since u = 5 and k = 102,

$$i = \mathrm{mod}(11 + 5, 5) + [11/5] \times 5 = 1 + 10 = 11$$

$$j = 1 \times 5 + 3 + (-1) \times [\{\mathrm{mod}(11, 5) + 1\}/2] = 5 + 3 - 1 = 7$$

which gives the address (11, 7). Likewise, there exists an equation that realizes the shuffling shown in Fig.23, along with various other equation that achieve various other shuffling formats.

The circuit that performs the above shuffling operations can be implemented in the configuration shown in Fig.24. In the figure, the reference numeral 46 designates a block address calculating circuit for calculating the block horizontal address (i) and the block vertical address (j) using the above given equations, and the block address obtained by the block address calculating circuit 46 is supplied to a write/read address generating circuit 45. On the basis of the supplied block address, the write/read address generating circuit 45 outputs a writw/read address to a RAM 44. In the RAM 44, each block is arranged according to the address, thus achieving the shuffling as shown in Figs.19, 21, 22, and 23.

Claims

1. A video signal encoding apparatus for compressing and encoding a digital video signal to obtain coded data compressed within a predetermined data amount, comprising:

   block structuring means (1,41) for structuring blocks each consisting of a plurality of pixels in said video signal;
   transformation means (2) for performing an orthogonal transform on each of the structured blocks to obtain a transform coeficient;
   quantizing means (4) for quantizing the transform coefficient;
   encoding means (5) for encoding the quantized data to obtain coded data;
   storage means (6), having a storage capacity approximately equal to said predetermined data amount, for storing the obtained coded data; and
   control means (8) for controlling the on-off operation of said encoding means on the basis of the amount of the coded data stored in said storage means,

   characterized by shuffling means (9) for shuffling the blocks structured by said block structuring means (1) so that said blocks may be sequentially supplied to said transformation means (2) starting with the blocks in the center of the screen.

2. A video signal encoding apparatus according to claim 1, characterized in that said control means (8) further controls the number of quantization bits for said quantizing means (4) on the basis of the amount of the coded data stored in said storage means.

3. A video signal encoding apparatus according to claim 1, characterized by

   decision means (43) for deciding the number of quantization bits for said quantizing means on the basis of the activity index of each block and the amount of the obtained coded data; and
   unit structuring means (41) for structuring units each comprising a plurality of block, prior to the orthogonal transform by said transformation means (2), by shuffling the blocks in such a manner that any given shuffling

block and four shuffling blocks most adjacent to said given shuffling block belong to different units.

4. A video signal encoding apparatus according to claim 1, characterized by

unit structuring means (41) for structuring units each comprising a plurality of blocks, prior to the orthogonal transform by said transformation means, by shuffling the blocks in such a manner that any given shuffling block and four shuffling blocks most adjacent to said given shuffling block belong to different units;
means (31,32) for obtaining the number of events, constituted by the zero run length and nonzero value of quantized data, by scanning the quantized data; and
decision means (14) for deciding the number of quantization bits for said quantizing means on the basis of the obtained number of events and the activity index of each block.

5. A video signal encoding apparatus according to claim 1, characterized by

means for cumulatively adding the code lengths of coded data, each code length being determined on the basis of the zero run length and nonzero value obtained by scanning the quantized data, and obtaining the quotient of the cumulative sum by the number of blocks; and
decision means (14) for deciding the number of quantization bits for said quantizing means (4) on the basis of the obtained quotient and the activity index of each block.

6. A video signal encoding apparatus according to claim 1, characterized by

unit structuring means (41) for structuring units each comprising a plurality of blocks, prior to the orthogonal transform by said transformation means, by shuffling the blocks in such a manner that any given shuffling block and four shuffling blocks most adjacent to said given shuffling block belong to different units;
means for predicting the amount of coded data to be obtained by encoding the quantized data; and event converting means (33) for converting events constituted by the zero run length and nonzero value of quantized data in accordance with the predicted amount of coded data; said encoding means (5) being provided for encoding data of each of the converted events to obtain coded data.

7. A video signal encoding apparatus as set forth in claim 6, characterized by means (32) for counting the number of events having a nonzero value whose absolute value is smaller than a predetermined value.

Patentansprüche

1. Vorrichtung zur Codierung eines Videosignals zur Kompression und Codierung von digitalen Videosignalen zum Erhalt codierter, innerhalb einer vorbestimmten Datenmenge komprimierter Daten, umfassend:

Block-Strukturierungs-Mittel (1, 41) zur Block-Strukturierung für strukturierte Blöcke, jeder bestehend aus einer Mehrzahl von Pixeln in dem Videosignal;
Transformations-Mittel (2) zur Durchführung einer Orthogonal-Transformation in jedem der strukturierten Blöcke, um Transformations-Koeffizienten zu erhalten;
Quantisierungs-Mittel (4) zur Quantisierung der Transformations-Koeffizienten;
Codierungs-Mittel (5) zur Codierung der quantisierten Daten um codierte Daten zu erhalten;
Menge zur Speicherung der erhaltenen codierten Daten; und
Steuerungs-Mittel (8) zur Steuerung der Ein-Aus-Operation der Codierungs-Mittel auf der Basis der codierten gespeicherten Datenmenge in dem Speicher-Mittel, gekennzeichnet durch,
Verschiebungs-Mittel (9) zur Verschiebung der strukturierten Blöcke, strukturiert durch die Block-Strukturierungs-Mittel (1), wobei die Blöcke nacheinander den Transformations-Mitteln (2) zugeführt werden, und mit dem Block in der Bildschirmmitte begonnen wird.

2. Vorrichtung zur Codierung eines Videosignals nach Anspruch 1, dadurch gekennzeichnet, daß die Steuerungs-Mittel (8) weiter die Anzahl der Quantisierungs-Bits für die Quantisierungs-Mittel (4) steuern, auf der Basis der codierten Datenmenge, die in den Speicher-Mitteln gespeichert ist.

3. Vorrichtung zur Codierung eines Videosignals nach Anspruch 1, gekennzeichnet durch,

Entscheidungs-Mittel (43) zur Entscheidung der Anzahl der Quantisierungs-Bits für die Quantisierungs-Mittel auf der Basis eines Aktivitätsindexes eines jeden Blocks und der erhaltenen codierten Datenmenge; und
Einheiten-Strukturierungs-Mittel (41) zur Strukturierung von Einheiten, wobei jede Einheit eine Mehrzahl von Blöcken aufweist, und zwar vor der Orthogonal-Transformation durch die Transformations-Mittel (2), indem die Blöcke so verschoben werden, daß zu jedem vorgegebenen Verschiebungsblock vier benachbarte Verschiebungsblöcke unterschiedlichen Einheiten angehören.

4. Vorrichtung zur Codierung eines Videosignals nach Anspruch 1, gekennzeichnet durch Einheiten-Strukturierungs-Mittel (41) zur Strukturierung von Einheiten, jede eine Mehrzahl von Blöcken umfassend, vor der Orthogonal-Transformation durch die Transformations-Mittel und durch Verschieben der Blöcke, in der Weise, daß ein vorgegebener Verschiebungsblock und vier die direkt benachbarten Verschiebungsblöcke zu diesem vorgegebenen Verschiebungsblock, unterschiedlichen Einheiten angehören;

Mittel (31, 32) zum Erhalt der Ereignisanzahl, gebildet durch die Null-Lauf-Länge und dem Ungleich-Null-Wert der quantisierten Daten durch Scannen der quantisierten Daten; und
Entscheidungs-Mittel (14) zur Entscheidung der Anzahl der Quantisierungs-Bits für die Quantisierungs-Mittel auf der Basis der erhaltenen Ereignisanzahl und des Aktivitätsindexes eines jeden Blocks.

5. Vorrichtung zur Codierung eines Videosignals nach Anspruch 1,

gekennzeichnet durch Mittel zur kumulierten Addition der Code-Längen der codierten Daten, wobei jede Code-Länge auf der Basis der Null-Lauf-Länge und des Ungleich-Null-Werts, erhalten durch Scannen der quantisierten Daten, bestimmt wird und durch Erhalt des Quotientens aus der kumulierten Summe der Blockanzahl und
Entscheidungs-Mittel (14) zur Entscheidung der Anzahl der Quantisierungs-Bits für die Quantisierungs-Mittel (4) auf der Basis des erhaltenen Quotientens und des Aktivitätsindexes eines jeden Blocks.

6. Vorrichtung zur Codierung eines Videosignals nach Anspruch 1, gekennzeichnet durch
Einheiten-Strukturierungs-Mittel (41) zur Strukturierung von Einheiten, jede eine Mehrzahl von Blöcken umfassend, vor der Orthogonal-Transformation durch die Transformations-Mittel, indem Blöcke in der Weise verschoben werden, daß jeder vorgegebene Verschiebungsblock und vier direkt benachbarte Verschiebungsblöcke zu dem vorgegebenen Verschiebungsblock, unterschiedlichen Einheiten angehören;

Mittel zur Vorbestimmung des Umfangs der codierten Daten, die durch Codierung der quantisierten Daten erhalten werden; und
Ereignis-Umwandlungs-Mittel (33) zur Umwandlung von Ereignissen, bestehend aus der Null-Lauf-Länge und dem Ungleich-Null-Wert der quantisierten Daten in Übereinstimmung mit dem vorherbestimmten Umfang der codierten Daten;
Codierungs-Mittel (5) zum Erhalt codierter Daten, vorgesehen zur Codierung von Daten eines jeden der konvertierten Ereignisse.

7. Vorrichtung zur Codierung eines Videosignals nach Anspruch 6, gekennzeichnet durch Mittel (32) zum Zählen der Anzahl der Ereignisse, die einen Ungleich-Null-Wert aufweisen und deren absoluter Wert kleiner als ein vorgegebener Wert ist.

Revendications

1. Dispositif de codage d'un signal vidéo pour comprimer et coder un signal vidéo numérique en vue d'obtenir des données codées, comprimées dans une quantité de données prédéterminée, comprenant :

des moyens (1, 41) de structuration de blocs pour structurer des blocs constitués chacun par une pluralité de pixels dans ledit signal vidéo ;
des moyens de transformation (2) pour appliquer une transformation orthogonale à chacun des blocs structurés pour obtenir un coefficient de transformation ;
des moyens de quantification (4) pour quantifier le coefficient de transformation ;

des moyens de codage (5) pour coder les données quantifiées pour obtenir des données codées ; de moyens de mémoire ayant une capacité de mémorisation à peu près égale à ladite quantité de données prédéterminée, pour mémoriser les données codées obtenues, et
des moyens de commande (8) pour commander l'opération d'activation-désactivation desdits moyens de codage sur la base de la quantité des données codées mémorisées dans lesdits moyens de mémoire ;

caractérisé par des moyens de mélange (9) pour mélanger les blocs structurés par lesdits moyens (1) de structuration de blocs de sorte que lesdits blocs peuvent être envoyés séquentiellement auxdits moyens de transformation (2) en commençant par les blocs situés au centre de l'écran.

2. Dispositif de codage de signal vidéo selon la revendication 1, caractérisé en ce que lesdits moyens de commande (8) commandent en outre le nombre de bits de quantification pour lesdits moyens de quantification (4) sur la base de la quantité des données codées mémorisées dans lesdits moyens de mémoire.

3. Dispositif de codage de signal vidéo selon la revendication 1, caractérisé par

des moyens de décision (43) pour décider du nombre de bits de quantification pour lesdits moyens de quantification sur la base de l'indice d'activité de chaque bloc et de la quantité des données codées obtenues ; et
des moyens (41) de structuration d'unités pour structurer des unités comprenant chacune une pluralité de blocs, avant la transformation orthogonale réalisée par lesdits moyens de transformation (2), par mélange des blocs de manière que n'importe quel bloc de mélange donné et quatre blocs de mélange directement les plus adjacents audit bloc de mélange donné appartiennent à des unités différentes.

4. Dispositif de codage de signal vidéo selon la revendication 1, caractérisé par

des moyens (41) de structuration d'unités pour structurer des unités comprenant chacune une pluralité de blocs, avant la transformation orthogonale réalisée par lesdits moyens de transformation (2), par mélange des blocs de manière que n'importe quel bloc de mélange donné et quatre blocs de mélange directement adjacents audit bloc de mélange donné appartiennent à des unités différentes ;
des moyens (31, 32) pour obtenir le nombre d'événements, constitués par la longueur d'exécution nulle et une valeur non nulle de données quantifiées, par exploration par balayage des données quantifiées ; et
des moyens de décision (14) pour décider du nombre de bits de quantification pour lesdits moyens de quantification sur la base du nombre obtenu d'événements et de l'indice d'activité de chaque bloc.

5. Dispositif de codage de signal vidéo selon la revendication 1, caractérisé par

des moyens pour réaliser l'addition cumulée des longueurs de code des données codées, chaque longueur de code étant déterminée sur la base de la longueur d'exécution nulle et d'une valeur non nulle obtenue par exploration par balayage des données quantifiées, et pour former le quotient de la somme cumulée, par le nombre de blocs ; et
des moyens de décision (14) pour décider du nombre de bits de quantification pour lesdits moyens de quantification (4) sur la base du quotient obtenu et de l'indice d'activité de chaque bloc.

6. Dispositif de codage de signal vidéo selon la revendication 1, caractérisé par

des moyens (41) de structuration d'unités pour structurer des unités comprenant chacune une pluralité de blocs, avant la transformation orthogonale réalisée par lesdits moyens de transformation, par mélange des blocs de manière que n'importe quel bloc de mélange donné et quatre blocs de mélange directement les plus adjacents audit bloc de mélange donné appartiennent à des unités différentes ;
des moyens pour prédire la quantité de données codées devant être obtenue par codage des données quantifiées ; et
des moyens (33) de conversion d'événements pour convertir des événements constitués par la longueur d'exécution nulle et la valeur non nulle de données quantifiées en fonction de la quantité prédite de données codées ;
lesdits moyens de codage (5) étant prévus pour le codage de données de chacun des événements convertis pour l'obtention de données codées.

7. Dispositif de codage d'un signal vidéo selon la revendication 6, caractérisé par des moyens (32) pour compter le nombre d'événements ayant une valeur non nulle et dont la valeur absolue est inférieure à une valeur prédéterminée.

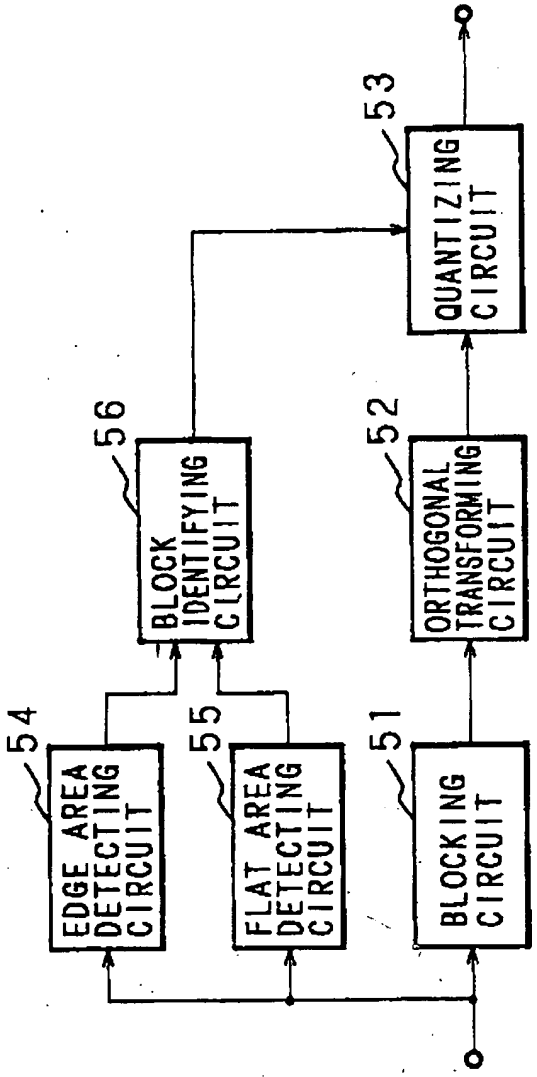


Fig. 1
Prior Art

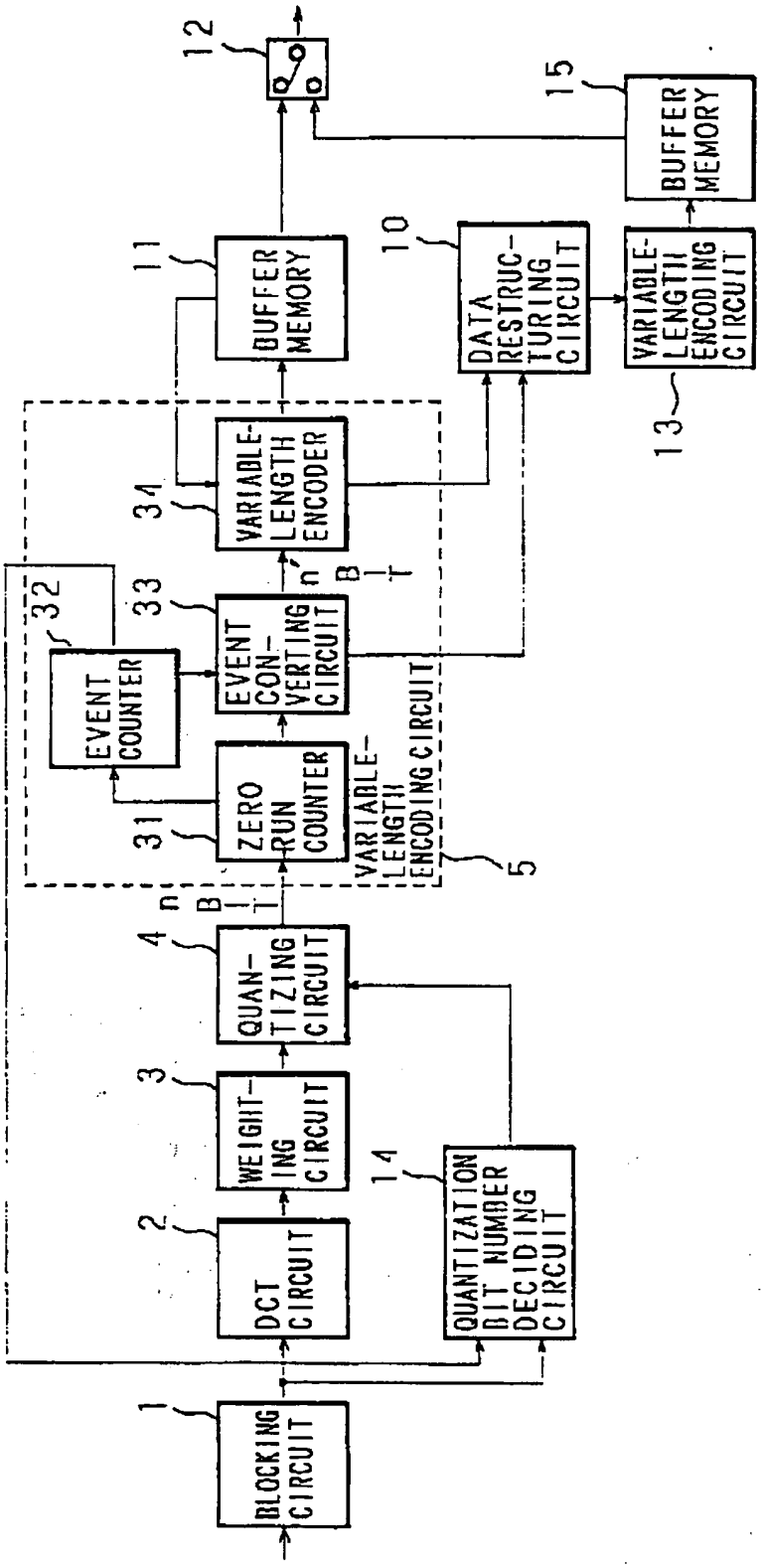
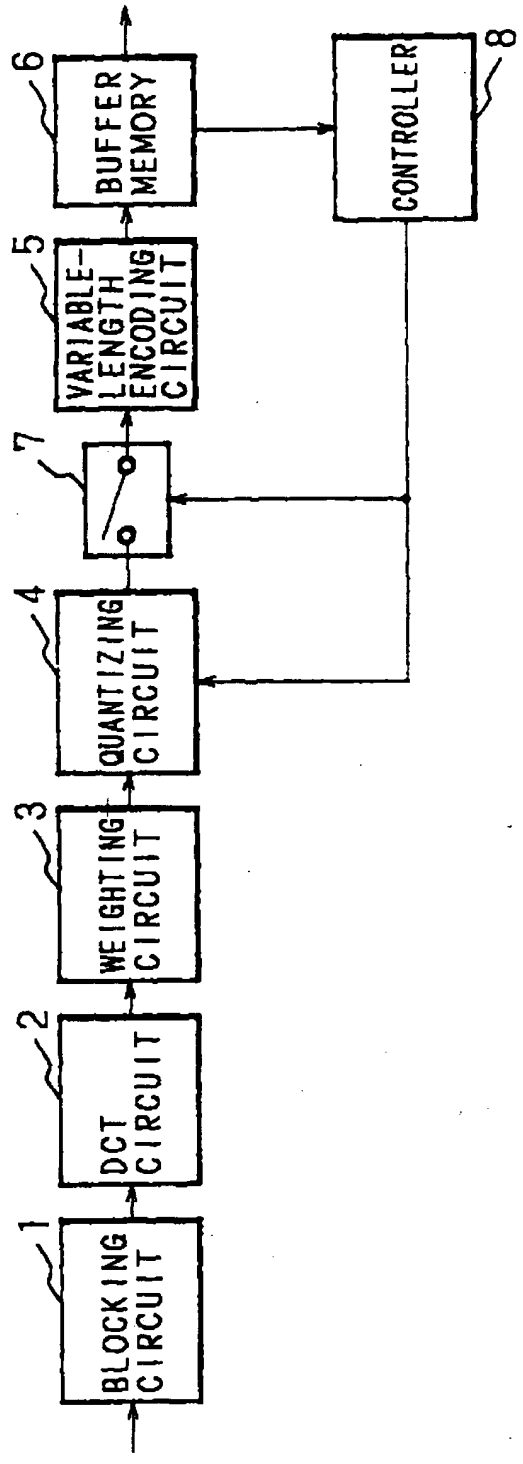

BLOCKING CIRCUIT
1
DCT CIRCUIT
2
WEIGHTING CIRCUIT
3
QUANTIZING CIRCUIT
4
n BIT
VARIABLE-LENGTH ENCODING CIRCUIT
5
ZERO RUN COUNTER
31
EVENT COUNTER
32
EVENT CONVERTING CIRCUIT
33
VARIABLE-LENGTH ENCODER
34
n' BIT
BUFFER MEMORY
11
DATA RESTRUCTURING CIRCUIT
10
VARIABLE-LENGTH ENCODING CIRCUIT
13
BUFFER MEMORY
15
12
QUANTIZATION BIT NUMBER DECIDING CIRCUIT
14

Fig. 9

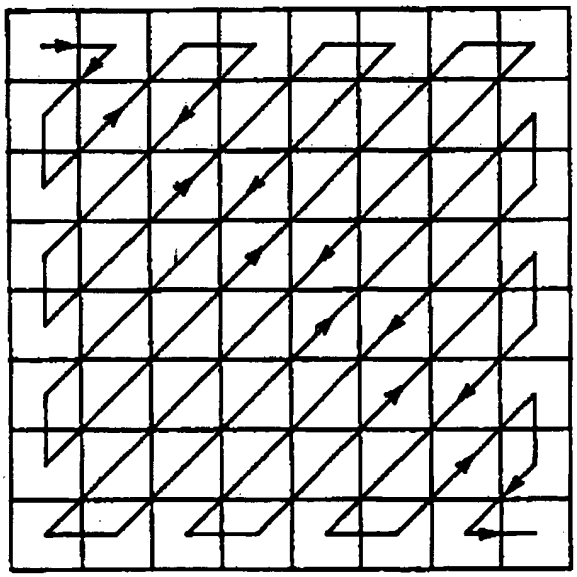

1
BLOCKING CIRCUIT
2
DCT CIRCUIT
3
WEIGHTING CIRCUIT
4
QUANTIZING CIRCUIT
7
5
VARIABLE-LENGTH ENCODING CIRCUIT
6
BUFFER MEMORY
8
CONTROLLER

F i g. 2

Fig. 3

80	3	0	2	1	0		
2	1	−1	0				
−1	0	1					
1	0						
0							

Fig. 4



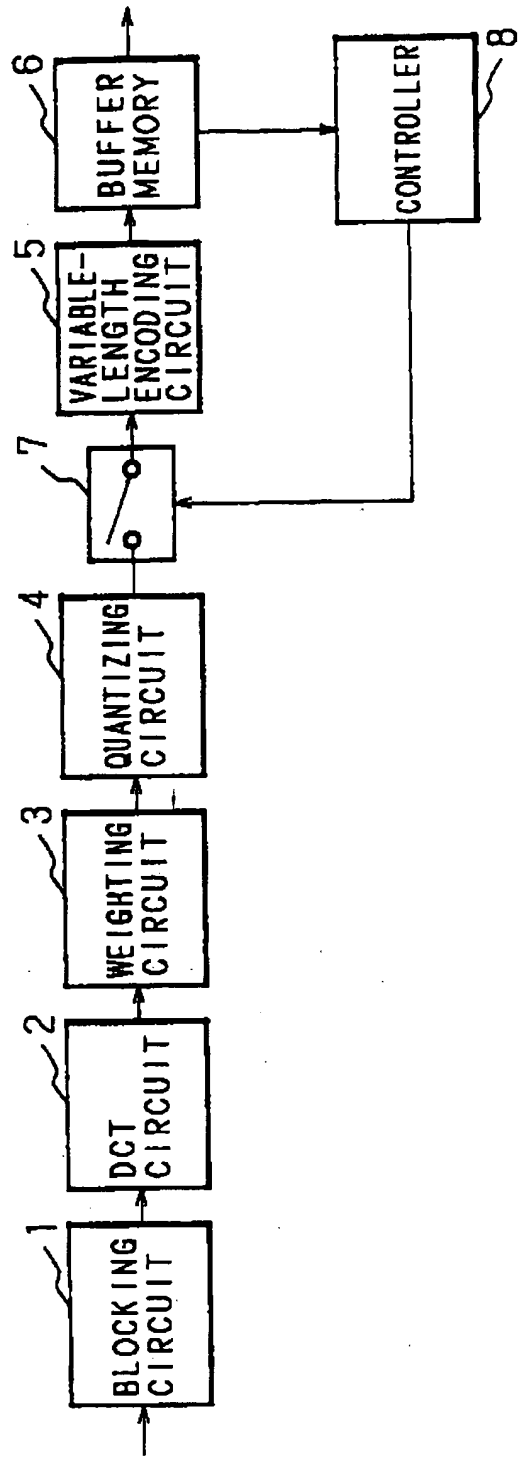

1
BLOCKING CIRCUIT
2
DCT CIRCUIT
3
WEIGHTING CIRCUIT
4
QUANTIZING CIRCUIT
7
5
VARIABLE-LENGTH ENCODING CIRCUIT
6
BUFFER MEMORY
8
CONTROLLER

Fig. 5

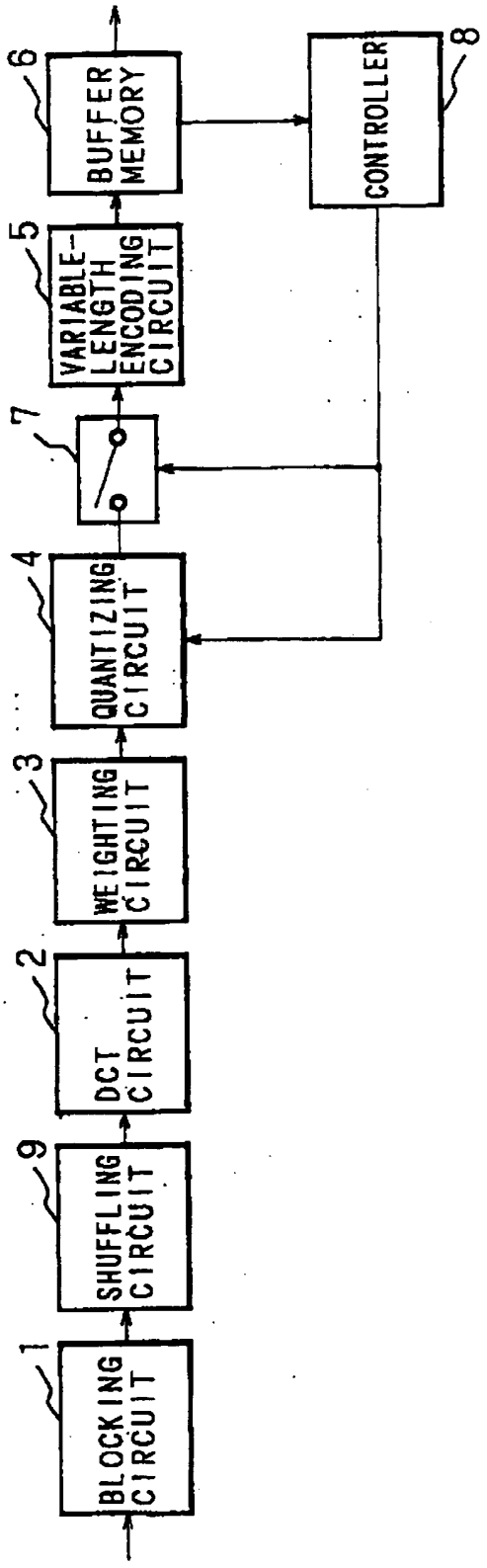

1
BLOCKING CIRCUIT
9
SHUFFLING CIRCUIT
2
DCT CIRCUIT
3
WEIGHTING CIRCUIT
4
QUANTIZING CIRCUIT
7
5
VARIABLE-LENGTH ENCODING CIRCUIT
6
BUFFER MEMORY
8
CONTROLLER

Fig. 6

Fig. 7(a)

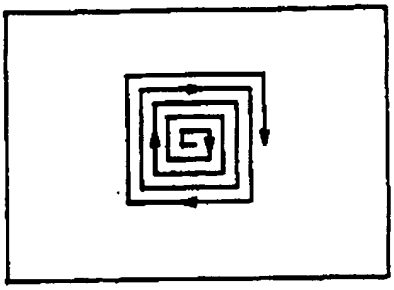


Fig. 7(b)

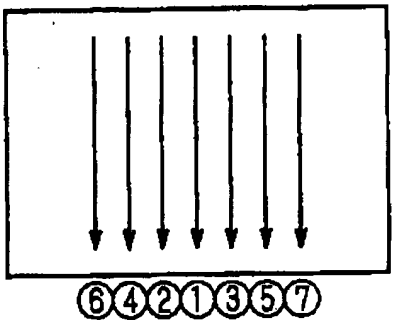


Fig. 7(c)

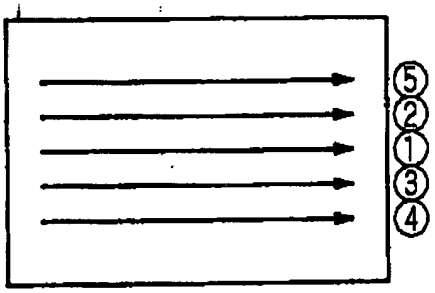
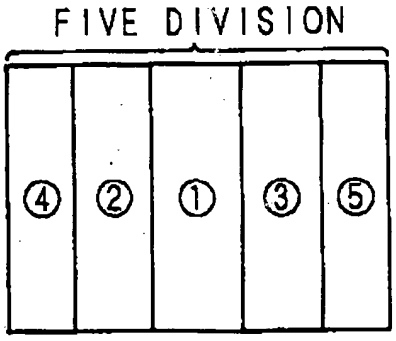


Fig. 7(d)



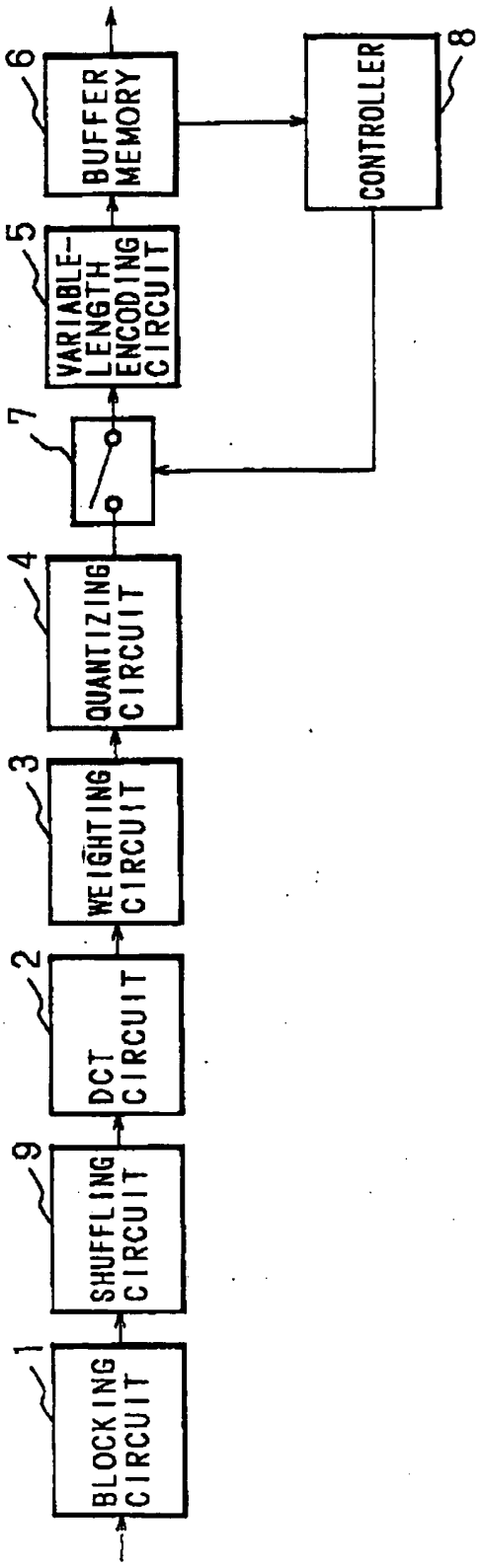

1
BLOCKING CIRCUIT
9
SHUFFLING CIRCUIT
2
DCT CIRCUIT
3
WEIGHTING CIRCUIT
4
QUANTIZING CIRCUIT
7
5
VARIABLE-LENGTH ENCODING CIRCUIT
6
BUFFER MEMORY
8
CONTROLLER

Fig. 8

Fig. 10

ACTIVITY INDEX \ USE PREDICTION OF BUFFER MEMORY 11	i	ii	iii	iv	v
a ~ b	9	8	8	7	7
b ~ c	8	8	7	7	6
c ~ d	8	7	7	6	6
d ~ e	7	7	6	6	6

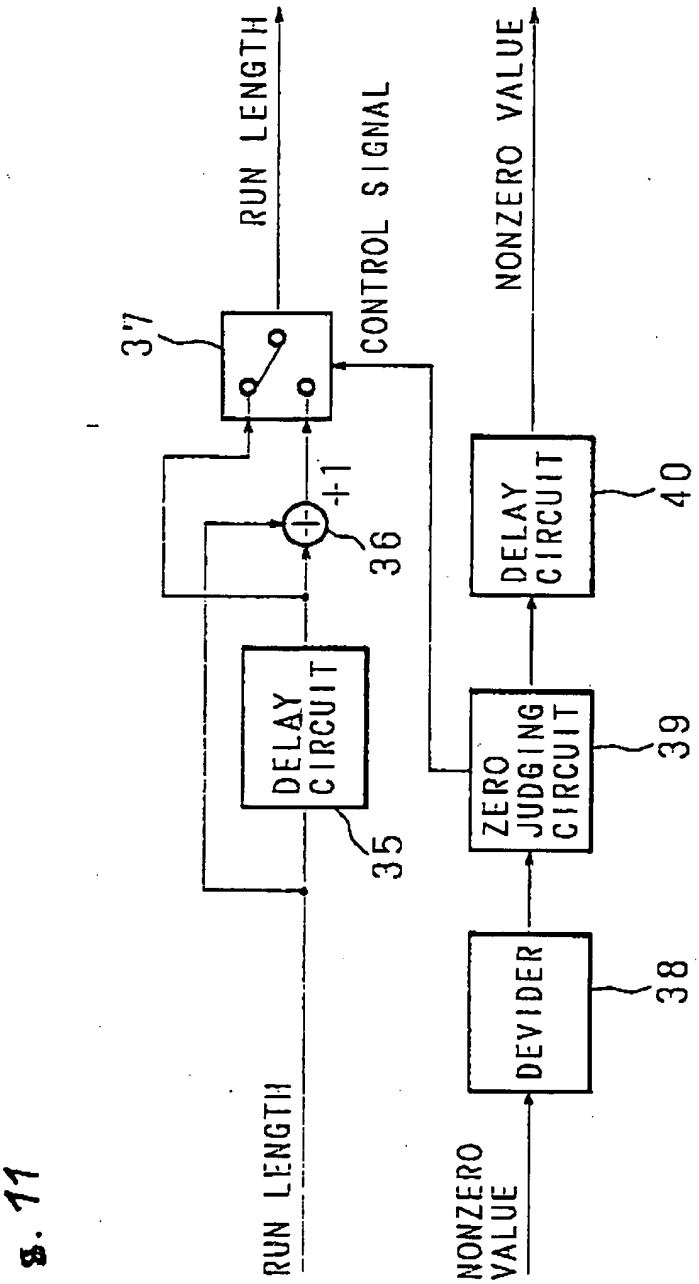

RUN LENGTH
CONTROL SIGNAL
NONZERO VALUE
37
-1
36
DELAY CIRCUIT
35
DELAY CIRCUIT
40
ZERO JUDGING CIRCUIT
39
DEVIDER
38
RUN LENGTH
NONZERO VALUE

Fig. 11

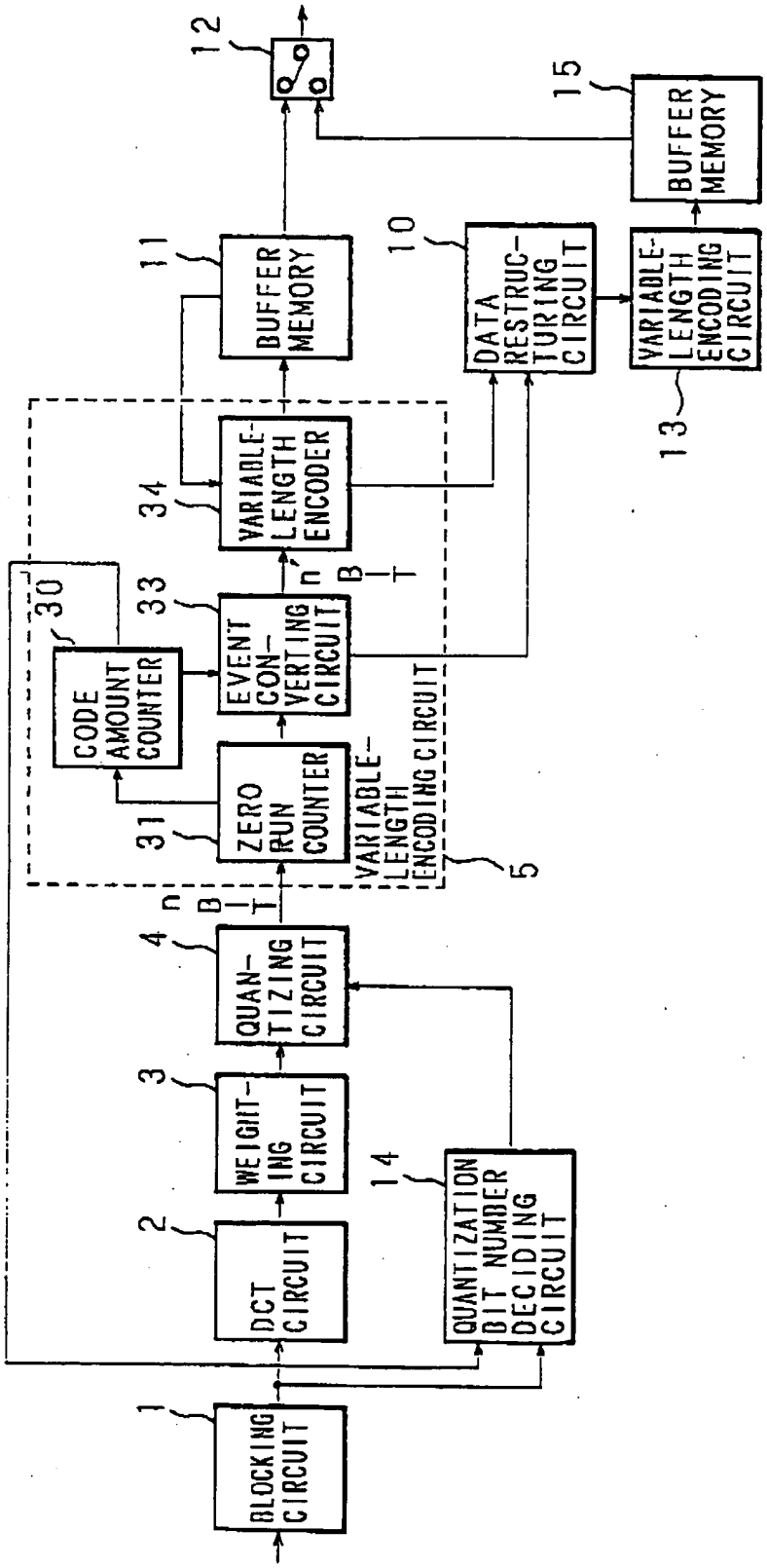

BLOCKING CIRCUIT
1
DCT CIRCUIT
2
WEIGHTING CIRCUIT
3
QUANTIZING CIRCUIT
4
n BIT
VARIABLE-LENGTH ENCODING CIRCUIT
5
ZERO RUN COUNTER
31
CODE AMOUNT COUNTER
30
EVENT CONVERTING CIRCUIT
33
n' BIT
VARIABLE-LENGTH ENCODER
34
BUFFER MEMORY
11
QUANTIZATION BIT NUMBER DECIDING CIRCUIT
14
DATA RESTRUCTURING CIRCUIT
10
VARIABLE-LENGTH ENCODING CIRCUIT
13
BUFFER MEMORY
15
12

FIG. 12

Fig.13

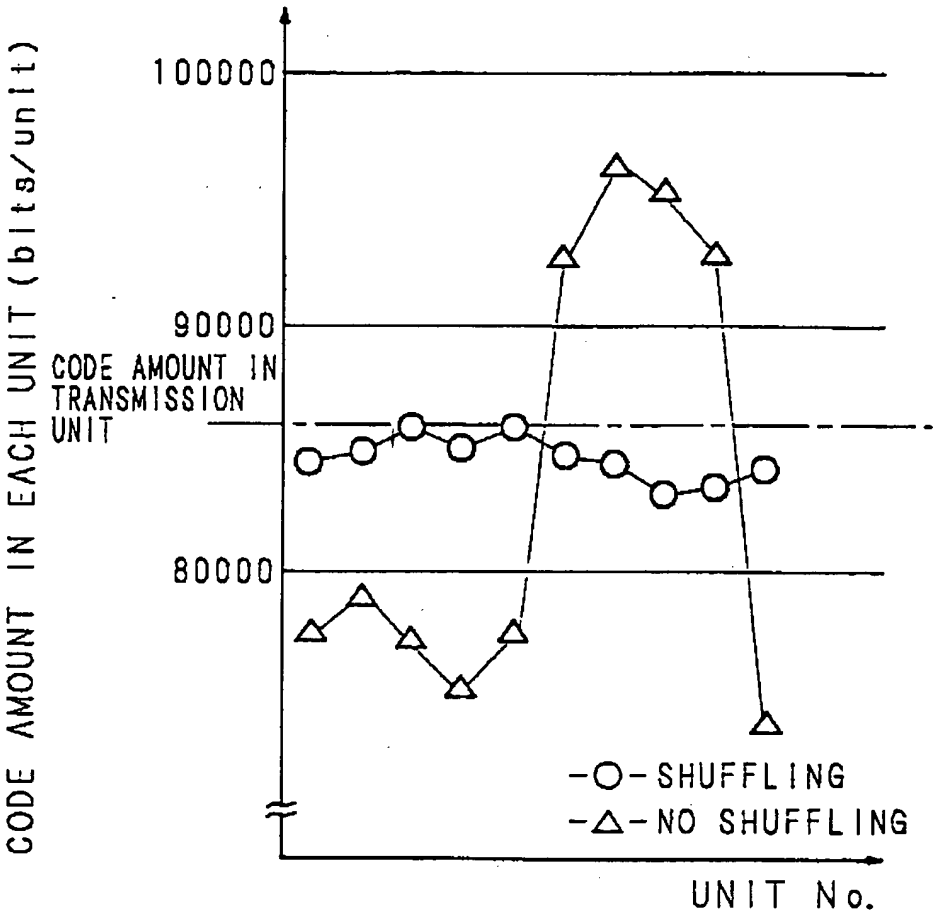

100000
90000
CODE AMOUNT IN TRANSMISSION UNIT
80000
CODE AMOUNT IN EACH UNIT (bits/unit)
-O- SHUFFLING
-△- NO SHUFFLING
UNIT No.

Fig. 14

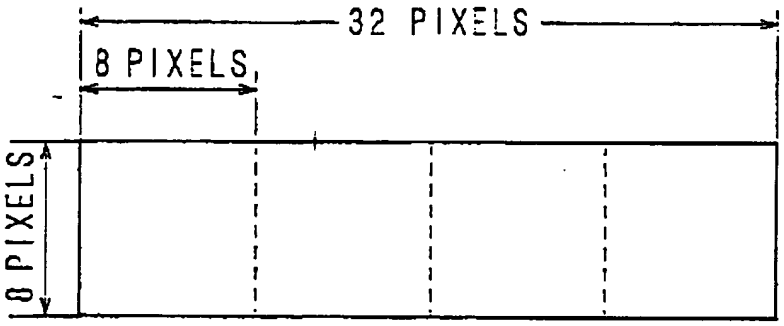
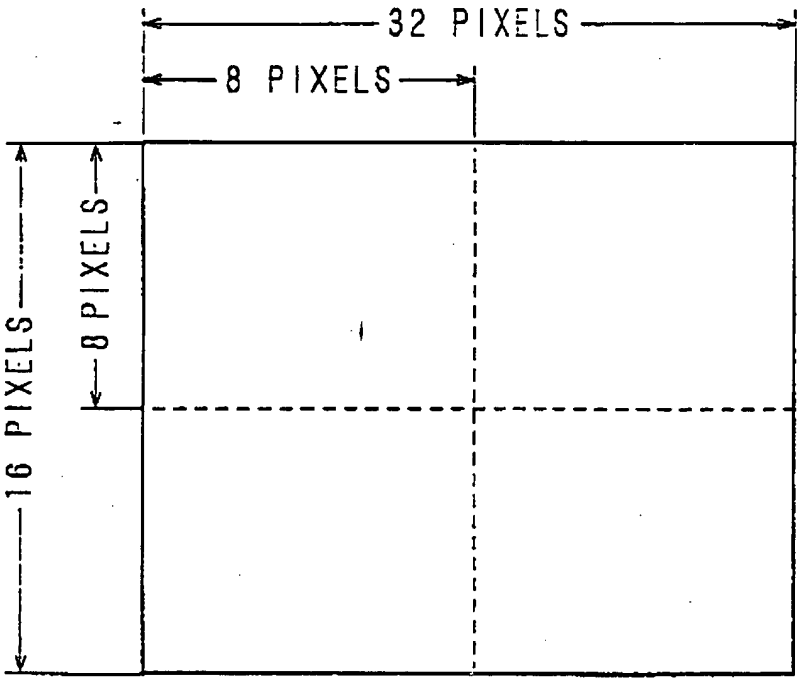


Fig. 15



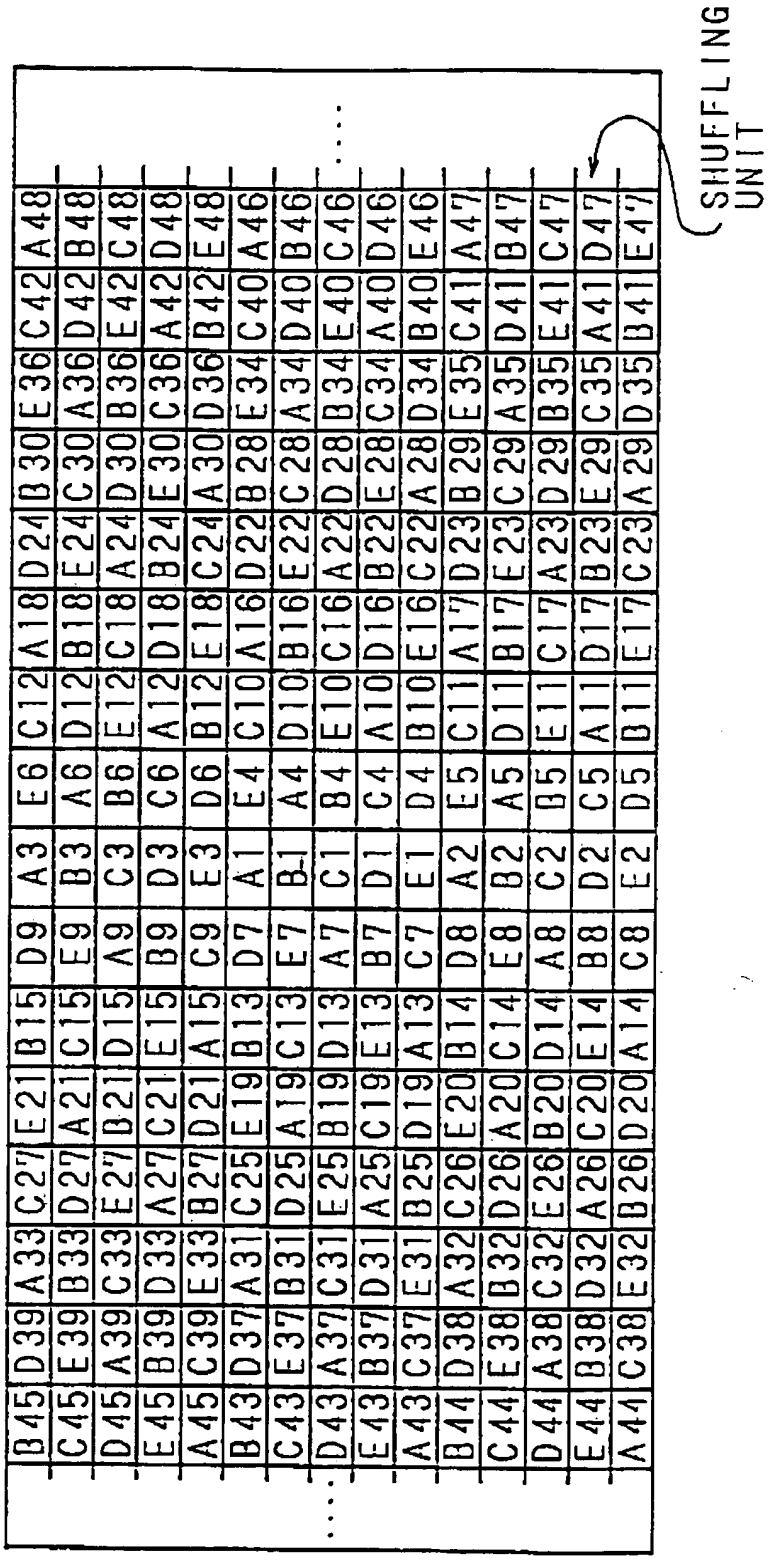
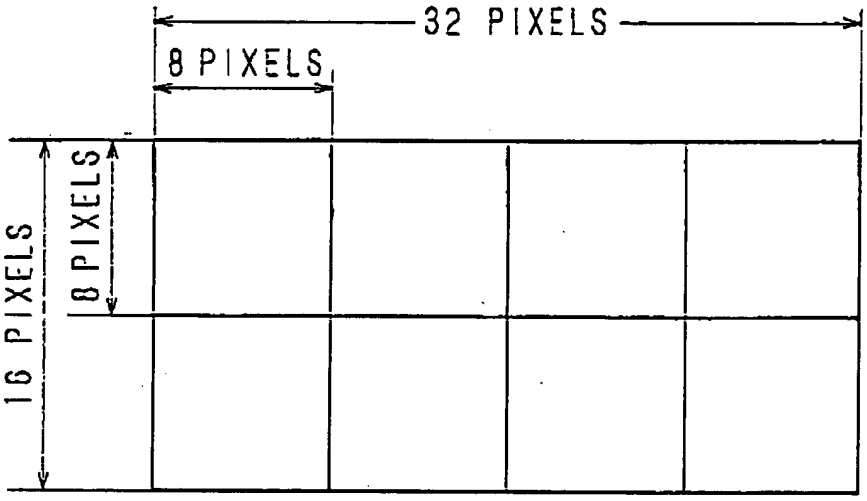

B45 D39 A33 C27 E21 B15 D9 A3 E6 C12 A18 D24 B30 E36 C42 A48
C45 E39 B33 D27 A21 C15 E9 B3 A6 D12 B18 E24 C30 A36 D42 B48
D45 A39 C33 E27 B21 D15 A9 C3 B6 E12 C18 A24 D30 B36 E42 C48
E45 B39 D33 A27 C21 E15 B9 D3 C6 A12 D18 B24 E30 C36 A42 D48
A45 C39 E33 B27 D21 A15 C9 E3 D6 B12 E18 C24 A30 D36 B42 E48
B43 D37 A31 C25 E19 B13 D7 A1 E4 C10 A16 D22 B28 E34 C40 A46
C43 E37 B31 D25 A19 C13 E7 B1 A4 D10 B16 E22 C28 A34 D40 B46
D43 A37 C31 E25 B19 D13 A7 C1 B4 E10 C16 A22 D28 B34 E40 C46
E43 B37 D31 A25 C19 E13 B7 D1 C4 A10 D16 B22 E28 C34 A40 D46
A43 C37 E31 B25 D19 A13 C7 E1 D4 B10 E16 C22 A28 D34 B40 E46
B44 D38 A32 C26 E20 B14 D8 A2 E5 C11 A17 D23 B29 E35 C41 A47
C44 E38 B32 D26 A20 C14 E8 B2 A5 D11 B17 E23 C29 A35 D41 B47
D44 A38 C32 E26 B20 D14 A8 C2 B5 E11 C17 A23 D29 B35 E41 C47
E44 B38 D32 A26 C20 E14 B8 D2 C5 A11 D17 B23 E29 C35 A41 D47
A44 C38 E32 B26 D20 A14 C8 E2 D5 B11 E17 C23 A29 D35 B41 E47
SHUFFLING UNIT

Fig. 16

Fig. 17



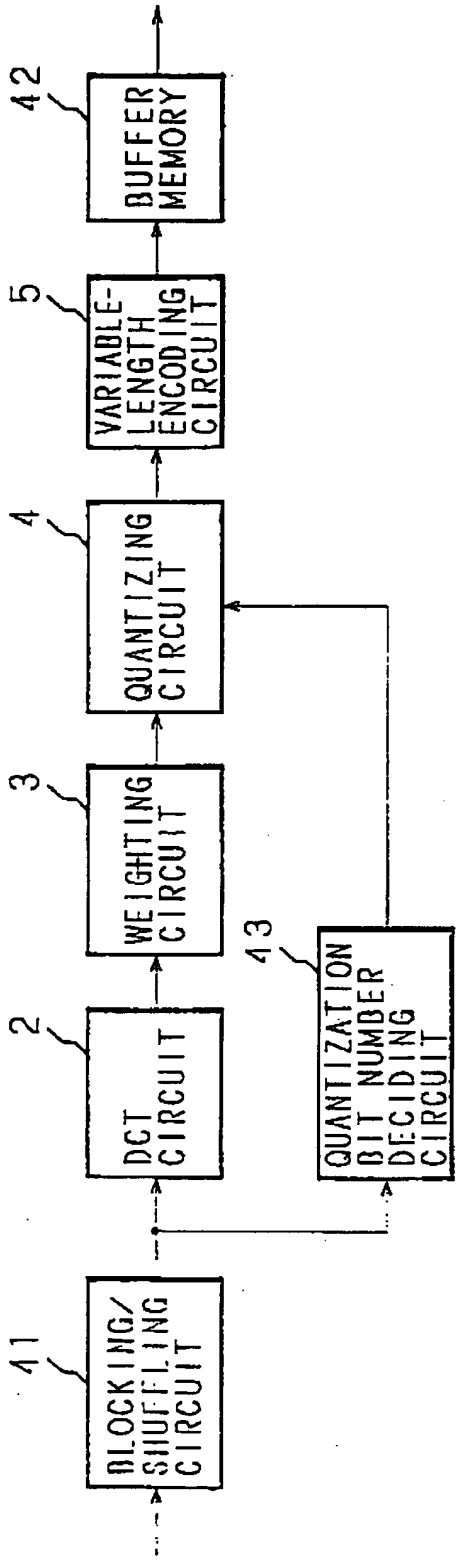

BLOCKING/ SHUFFLING CIRCUIT
41
DCT CIRCUIT
2
WEIGHTING CIRCUIT
3
QUANTIZING CIRCUIT
4
VARIABLE-LENGTH ENCODING CIRCUIT
5
BUFFER MEMORY
42
QUANTIZATION BIT NUMBER DECIDING CIRCUIT
13

FIG. 18

FIG. 19

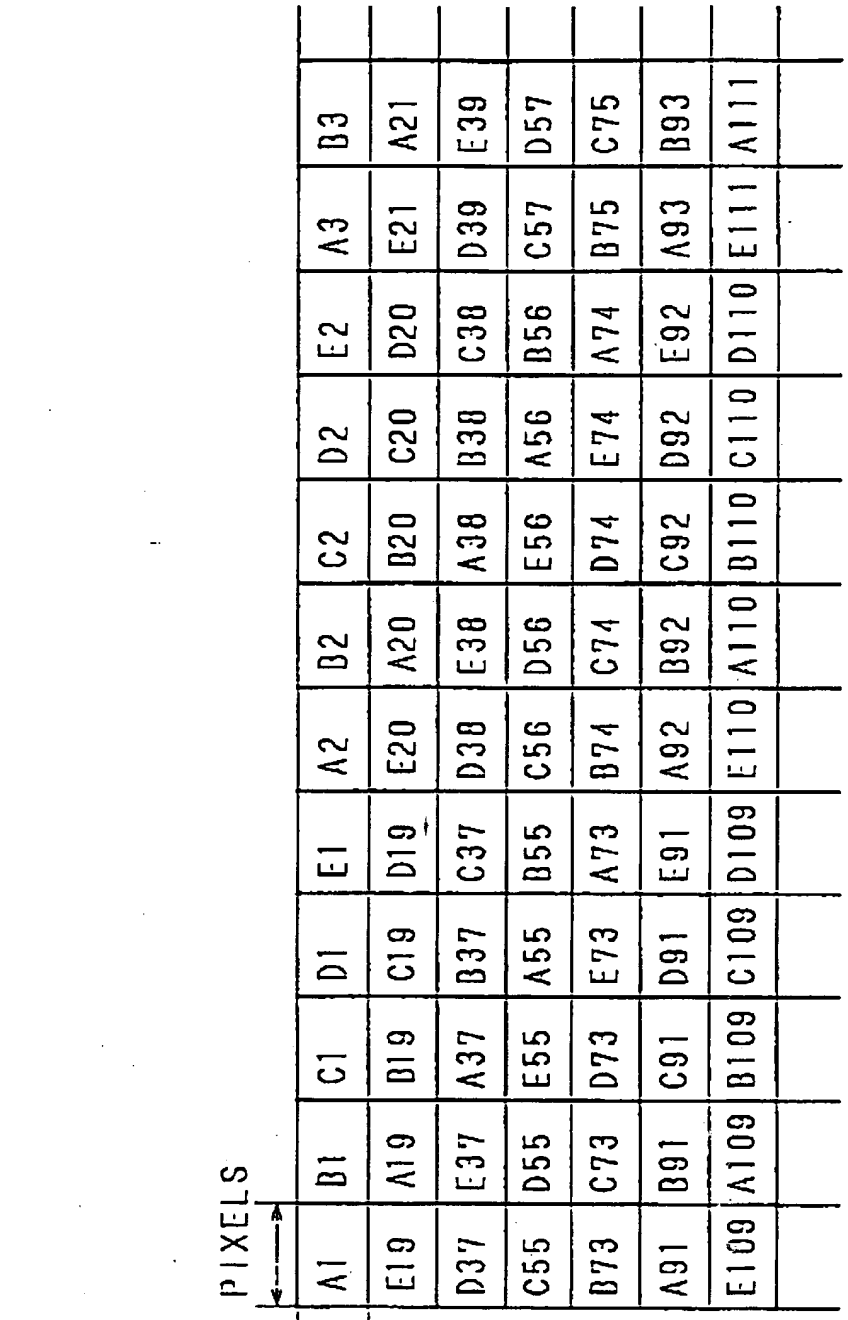
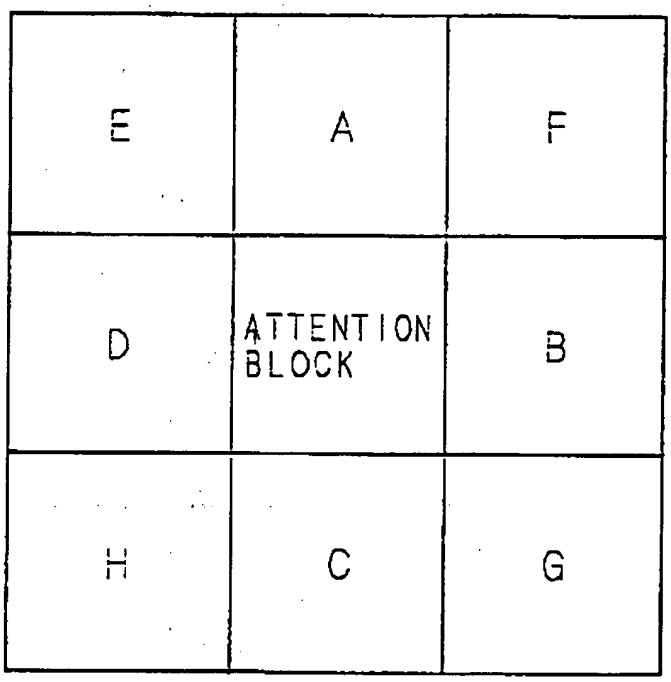

n PIXELS
n PIXELS
A1 B1 C1 D1 E1 A2 B2 C2 D2 E2 A3 B3
E19 A19 B19 C19 D19 E20 A20 B20 C20 D20 E21 A21
D37 E37 A37 B37 C37 D38 E38 A38 B38 C38 D39 E39
C55 D55 E55 A55 B55 C56 D56 E56 A56 B56 C57 D57
B73 C73 D73 E73 A73 B74 C74 D74 E74 A74 B75 C75
A91 B91 C91 D91 E91 A92 B92 C92 D92 E92 A93 B93
E109 A109 B109 C109 D109 E110 A110 B110 C110 D110 E111 A111

Fig. 20



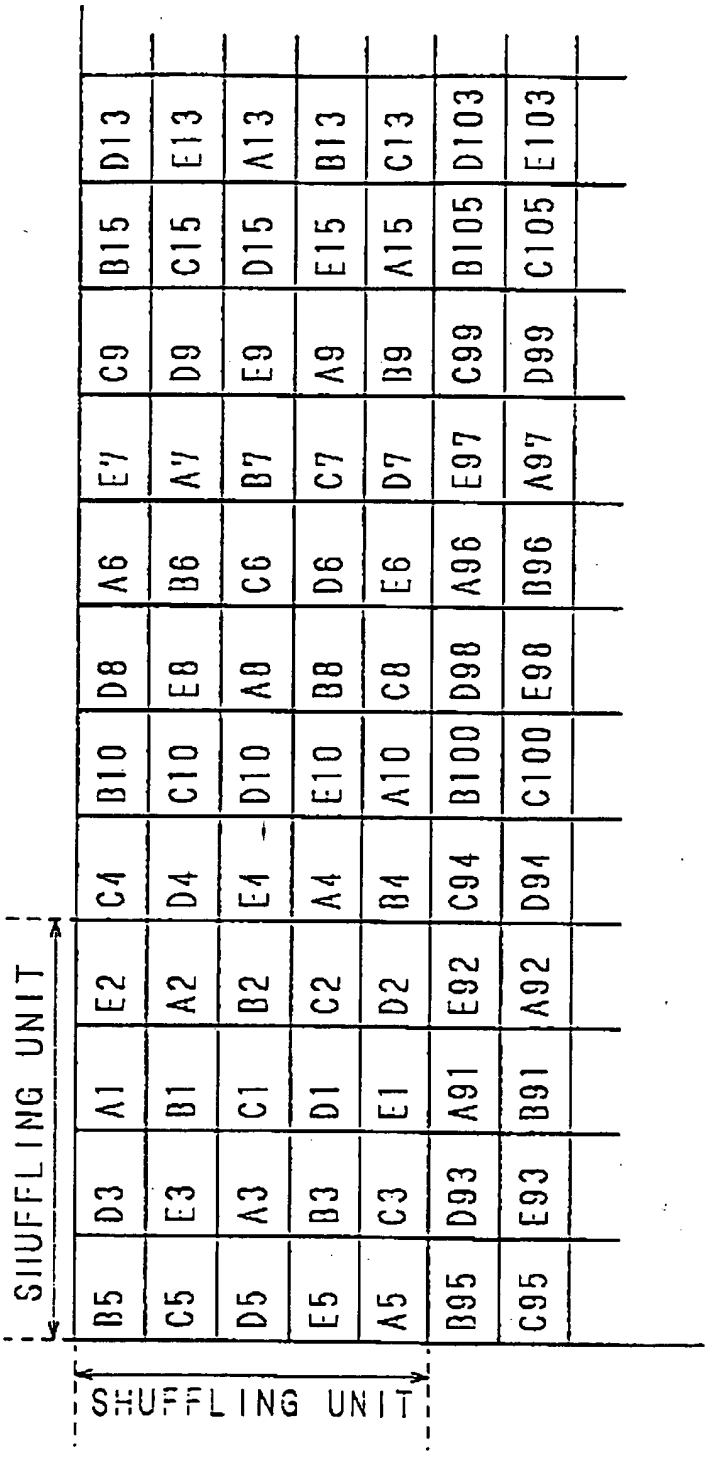

SHUFFLING UNIT
SHUFFLING UNIT
B5 D3 A1 E2 C4 B10 D8 A6 E7 C9 B15 D13
C5 E3 B1 A2 D4 C10 E8 B6 A7 D9 C15 E13
D5 A3 C1 B2 E4 D10 A8 C6 B7 E9 D15 A13
E5 B3 D1 C2 A4 E10 B8 D6 C7 A9 E15 B13
A5 C3 E1 D2 B4 A10 C8 E6 D7 B9 A15 C13
B95 D93 A91 E92 C94 B100 D98 A96 E97 C99 B105 D103
C95 E93 B91 A92 D94 C100 E98 B96 A97 D99 C105 E103

FIG. 21

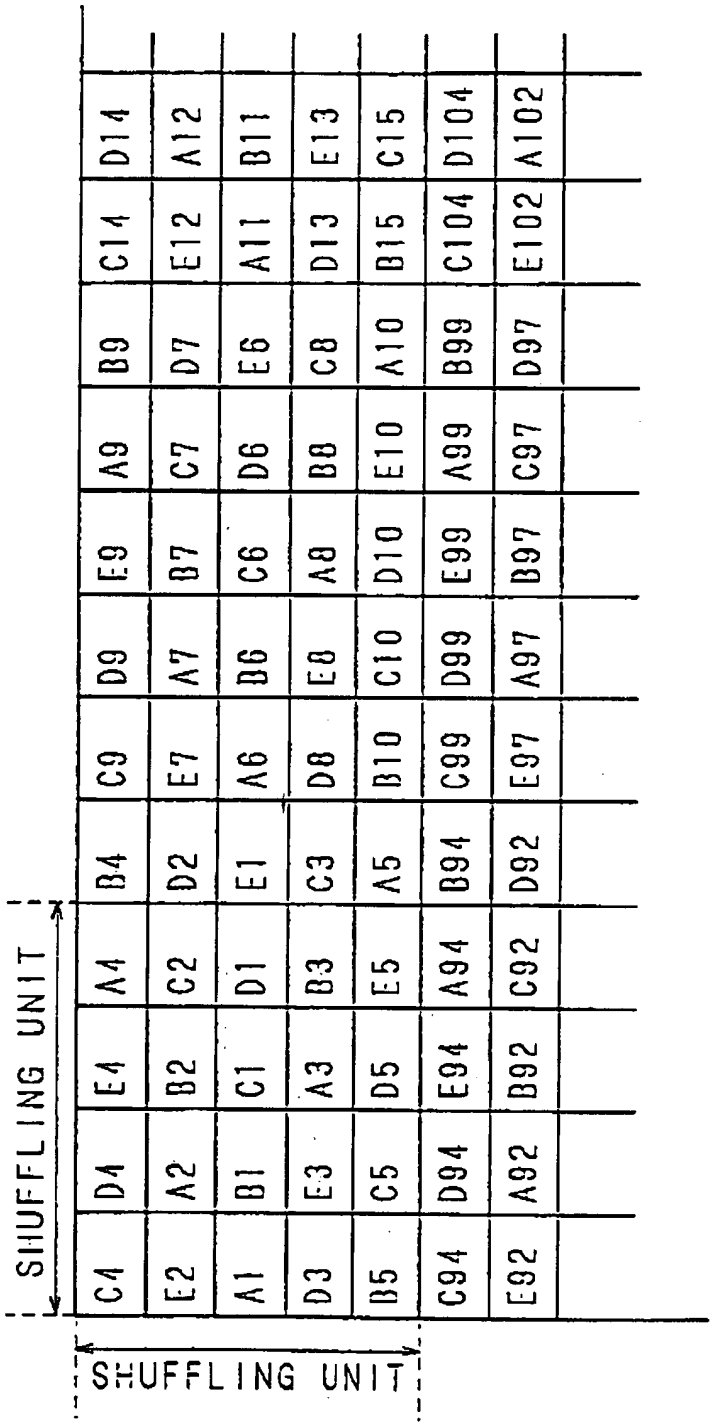

SHUFFLING UNIT
SHUFFLING UNIT
C4 D4 E4 A4 B4 C9 D9 E9 A9 B9 C14 D14
E2 A2 B2 C2 D2 E7 A7 B7 C7 D7 E12 A12
A1 B1 C1 D1 E1 A6 B6 C6 D6 E6 A11 B11
D3 E3 A3 B3 C3 D8 E8 A8 B8 C8 D13 E13
B5 C5 D5 E5 A5 B10 C10 D10 E10 A10 B15 C15
C94 D94 E94 A94 B94 C99 D99 E99 A99 B99 C104 D104
E92 A92 B92 C92 D92 E97 A97 B97 C97 D97 E102 A102

FIG. 22

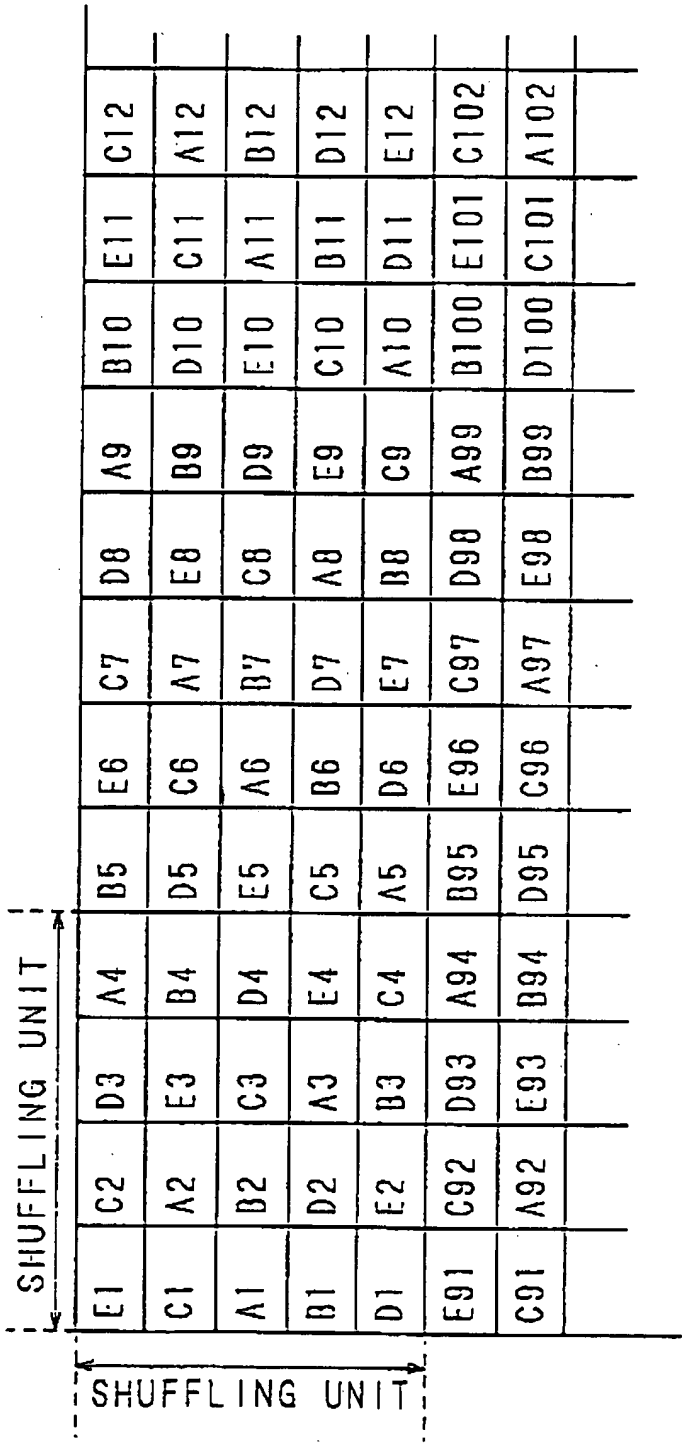
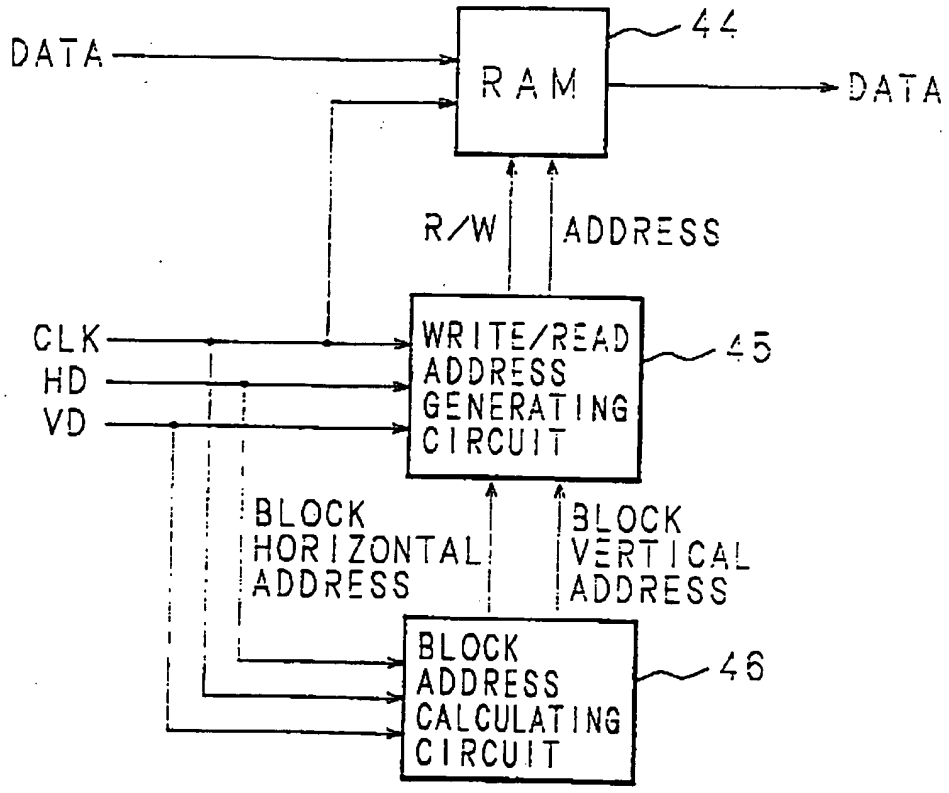

SHUFFLING UNIT
SHUFFLING UNIT
E1 C2 D3 A4 B5 E6 C7 D8 A9 B10 E11 C12
C1 A2 E3 B4 D5 C6 A7 E8 B9 D10 C11 A12
A1 B2 C3 D4 E5 A6 B7 C8 D9 E10 A11 B12
B1 D2 A3 E4 C5 B6 D7 A8 E9 C10 B11 D12
D1 E2 B3 C4 A5 D6 E7 B8 C9 A10 D11 E12
E91 C92 D93 A94 B95 E96 C97 D98 A99 B100 E101 C102
C91 A92 E93 B94 D95 C96 A97 E98 B99 D100 C101 A102

FIG. 23

Fig. 24


DATA
RAM
44
DATA
R/W
ADDRESS
CLK
HD
VD
WRITE/READ
ADDRESS
GENERATING
CIRCUIT
45
BLOCK
HORIZONTAL
ADDRESS
BLOCK
VERTICAL
ADDRESS
BLOCK
ADDRESS
CALCULATING
CIRCUIT
46